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Simulation Models for Variable Speed Electric Drives

by

RAJAT BHARGAVA ©

A Thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for a degree of

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Em Bocancea

Mr. Emanuel Bocancea

ABSTRACT

This thesis describes simulation models for assessing the performance of variable speed power electronic drive systems. Simulation models are developed for both the Voltage Source Inverter (VSI) and the Current Source Inverter (CSI) using SPICE3. A simulation model for a complete drive system is presented for a VSI drive system using a 12-pulse input rectifier and a 3-level Pulse width modulation (PWM) VSI.

Models are described for simulating the action of the input, output and load portions of both the CSI and VSI drive types. The drive systems are discussed with reference to both 6-pulse and 12-pulse rectifier stages. The 12-pulse rectifier input stage uses a Δ-Δ / Δ-Y transformer. The modeling of a Δ-Δ / Δ-Y transformer is done using d-q axis theory. DC Filters are used to obtain a ripple free dc voltage or current, which acts as the input to the inverter stage. Pulse width modulation (PWM) is used to control the inverter output stage of both drive systems. The induction motor acts as the load to the inverter output stage and is also modeled using d-q axis theory. Experimental results are used to verify that the simulation models are accurate and represent the real system. The simulation models are constructed using actual drive parameters obtained by performing various experimental tests. The performance of a low distortion rectifier is investigated using both simulation and experimental data, with emphasis on the current harmonics, the power factor and the total harmonic distortion. The result of this performance analysis shows that the novel rectifier topology can be used to successfully lower the total harmonic distortion of the rectifier input line current whilst achieving a unity power factor.

The various simulation techniques developed in this work are implemented using SPICE3 and lower the difficulty of simulating an entire drive topology. Fast run times are obtained as a result and convergence problems are improved. Close agreement of the simulation results with experimental ones prove the accuracy of the SPICE3 models.

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LIST OF SYMBOLS

SPICE	Simulation Program with Integrated Circuit Emphasis
ac	alternate current
VSI	Voltage Source Inverter
CSI	Current Source Inverter
PWM	Pulse Width Modulation
DPF	Displacement Power factor
THD	Total Harmonic Distortion
CDF	Current Distortion Factor
PF	Power Factor
A	Nodal admittance matrix
RELTOL	Relative Tolerance
ABSTOL	Absolute Tolerance
I_a	Phase A Current
L_m	Magnetizing inductance
L_{ls}	Stator inductance
$V_{a,ph}$	Phase A Voltage
LABVIEW	Laboratory Virtual Instrument Engineering Workbench
GPIB	General Purpose Interface Bus
d-axis	direct axis
q-axis	quadrature axis
SCR	Silicon Controlled Rectifier
kVA	Kilovolt Amperes
GTO	Gate Turn-off Thyristor
NPC	Neutral Point Clamped
IM	Induction Motor
ω	angular frequency

I_d	dc-link current
V/f	volts per hertz
ψ	induction motor flux linkage
T_e	electromagnetic torque
T_L	load torque
ϕ_{ag}	air-gap flux
f_{sl}	slip frequency
L_s	source inductance
PCC	Point of Common Coupling
I_1	fundamental current
ϕ	phase angle
I_{ca}	Phase A capacitor current

Chapter 1

INTRODUCTION

The ac variable speed drive is a complex non-linear system. The computer simulation and modeling becomes essential for the analysis and design of such a system. SPICE3, which is the simulation software used in this work, has now become a widely accepted circuit simulation package for Power Electronic circuits. To develop a model for an electric drive system in SPICE3 is to widen its capabilities by simulating the whole drive system in only one simulation. This avoids complex mathematical operations for its performance analysis, making drive design more straightforward and practical.

Computer aided circuit simulation of power electronic systems offer the system designer the opportunity to explore all the various design trade-off and options and also to perform wide-ranging comparative investigation, optimization and performance analysis.

1.1 Drive Topologies

This work discusses two basic drive topologies - the Voltage Source Inverter [1]-[3] and the Current Source Inverter [4], [5]. These two drives are the most common drives used in the industry. Simulation models for these drives facilitates the comparative analysis and design of new drive topologies.

The rectifier stage of a drive is commonly either a 6-pulse diode bridge rectifier or a 12-pulse diode bridge rectifier [6], [7]. For the 12-pulse rectifier the input stage is a Δ-Δ, Δ-Y transformer with the output voltages of the transformer phase shifted by 30° from each other. The series connection of two 6-pulse diode bridge rectifier connected to such a transformer gives a 12-pulse operation which is applicable for high power applications.

The dc-link filter stage is a large capacitor for the VSI so that the input to the

inverter is an approximately constant dc voltage. The voltage source inverter can be either a square wave inverter or a pulsewidth modulated (PWM) inverter. The rectifier stage to the square wave inverter is a phase controlled rectifier to control the input dc voltage. The PWM inverter has the provision of control of the output voltage and hence can be supplied from a fixed dc voltage, see Fig.1.1. The PWM VSI inverter uses high switching frequency to eliminate the dominant harmonics in the output line-to-line voltage. The simulation of such high frequency operation makes analysis simpler.

The dc-link filter for a CSI drive is a large inductor in the dc rail which results in a stiff dc current being fed to the inverter, see Fig.1.2. Current fed into the inverter is converted into three ac line currents by the appropriate PWM gating pattern of the inverter switches see section 5.1.1. Current harmonics are absorbed by the output filter so as to provide sinusoidal load current and voltage. A generalized structure of a simple controller for a current source inverter is also explained.

The output of a drive topology is the induction motor. For the control of induction motors, a fixed frequency ac supply with variable voltage or a variable frequency ac supply with variable voltage or current is required. Variable speed drives utilizing an ac motor fed with variable frequency, three-phase ac derived from an inverter, are encountered with increasing frequency [4]. A simulation model for the induction motor helps to examine both the transient and steady state.

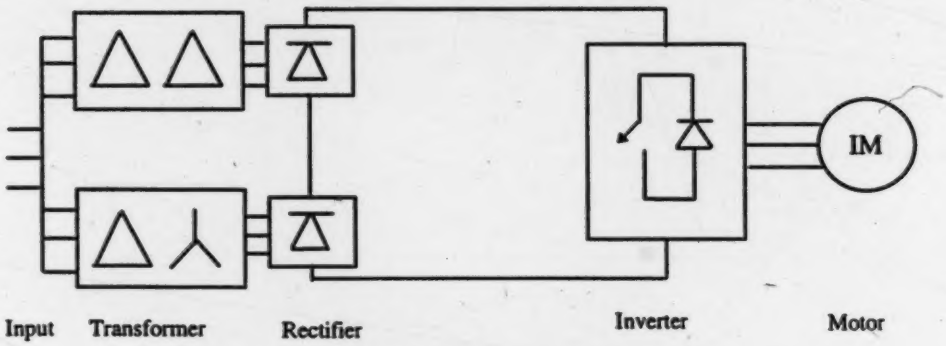


Fig. 1.1 Block diagram for PWM VSI Inverter Drive

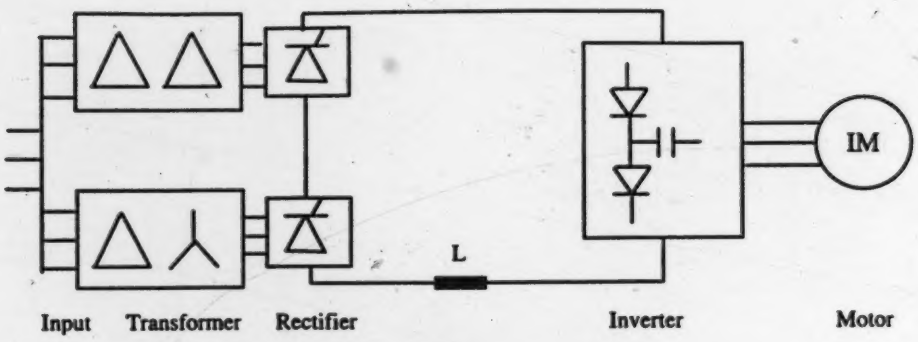


Fig. 1.2 Block diagram for PWM CSI Inverter Drive

1.2 SPICE3 simulation and experimental results

SPICE is a standard circuit simulator program used by the electronic industry. This program uses non-linear physical models to simulate semiconductor components. In power electronics these micromodels are useful at the switch level of simulation wherein the commutating performance of the power switch in the circuit is of main interest. Because, at this level events occur in a very short time interval as compared with the total on or off state of the device, decoupling is usually possible. This decoupling allows a local simulation of the switches [2].

The simulation software used in this work is SPICE3 (Version 3f4). The simulator is equipped with a schematic capture input program and postprocessor for waveform analysis. The previous versions of SPICE primarily used the voltage controlled and current controlled switch for modeling and simulation [48]. In most of the models the total system ends up having a large number of switches, thus requiring larger amount of memory and long computation times. In the latest version of SPICE3 (version 3f4), the "B" and "U" statements introduced can be used to more effectively model switches and control circuit transfer functions used in power electronic drive systems. These B-statement and U-statement can be used as voltage function and current functions defining various complex equations. Thus, the flexibility and capability of SPICE as a stand alone program can be enhanced while significantly reducing run times.

The new features of SPICE3 are used very effectively for the simulation of various power electronic circuits [9]. The modeling of the Δ-Δ, Δ-Y transformer is done using d-q axis theory. In this theory the time varying parameters are eliminated and the variables and parameters are expressed in orthogonal or mutually decoupled direct (d) and quadrature (q) axes. The B-statement is used to model the complex equations resulting from the transformation. The modeling of the induction machine is also done in the same manner using d-q axis theory.

The diode rectifier topology uses the simple power diode from the SPICE3 device library. For better accuracy, such as for the simulation of the novel rectifier topology the device parameters can be altered. The switching device in the case of a square wave inverter is modeled by using a B-statement in series with a diode.

SPICE3 becomes very effective when modeling the inverter topology. At high switching frequency operations, as in the case of PWM inverters simulation has convergence problems due to fast transfer of current from one switching device to the other. The B-statement solves this problem by modeling the inverter legs by three B-statements representing the switching pattern of the six devices. This also reduces the number of switching devices.

In the present work, SPICE3 is used for generating the raw data for all the simulated waveforms and the raw data is postprocessed using Excel to obtain the waveform plots. Harmonic analysis is also done using SPICE3. In addition, SPICE3 is provided with the Interactive Interpreter that helps to monitor parameters in a single run by means of a do loop. This feature is used to generate the data for the various performance curves for the novel rectifier topology.

All the parameters values used in the SPICE3 model are the same as that used in the experimental setup. For the Δ-Δ, Δ-Y transformer, the Open Circuit test and the Short Circuit test is done to determine the parameter values. Similarly, for the induction motor the Load test , the Standstill test and the Stator dc test is done. This helps in a logical comparison of the simulation and experimental results.

The data used for the experimental waveforms was generated using a data acquisition system called LABVIEW - Laboratory Virtual Instrument Engineering Workbench. The experimental measurement system consists of the following: Tektronix TDS 420 four channel oscilloscope, Power Macintosh 7100/66 computer running LABVIEW 4.0 software, GPIB card NI-488, GPIB cable, high voltage probe isolators with scaling factor of 1/500 and 1/50, clamp-on Hall-effect current probe isolator with scaling factor of 100mV/A and 10mV/A.

1.3 Literature Survey

Numerous digital and analogue computer simulation studies of the performance of electrical drives have been done in the past [10]-[14]. However, because of the complexity of power electronic circuits, the vast majority of these studies have neglected the power-electronic circuit topology and assumed a zero impedance source, with the power electronic switching action represented solely by the theoretical voltages (currents) supplied to the drive motor.

Digital computer simulation studies [15],[16] which have attempted to take into account the power-electronic circuits and source impedance effects, for example input rectifier, dc link filter, inverter, etc. have all involved significant simplifying assumptions and therefore provides a very limited, albeit useful first approximation to the various interactions.

The power and flexibility of power electronic circuit simulation depends heavily on the CAD package library of power electronic devices and components available to the user. To specialize these CAD packages for PWM inverter drive system requires an additional range of library models to represent devices, components, machines and processes specific to power electronic systems to be developed [17], [18].

A PC based simulation CAD tool, PECADS is proposed in [19]. It uses real structure simulation (RSS) and digital identification for power electronic computer aided design and simulation. The simulation package follows the RSS rule that each

block has to be simulated in such a manner that the output signals will represent the same evolution as the real ones.

Another power electronic CAD package has been proposed in [19] which has been specially designed to cater for the simulation of pulse-width modulation controlled power electronic systems. This CAD package combines the features and facilities of a previously developed PWM generation and analysis package called PWLIB [20] with a circuit analysis package called BTRAP. The "equivalent-circuit" electromechanical induction motor model, which, when incorporated into the PWLIB/BTRAP package, provides the CAD facilities for developing various integrated drive systems.

A flexible method to design a complete three-phase inverter drive is to use a circuit simulator like SABER, but a serious problem is that designing a complete three-phase inverter, especially operating at low fundamental frequency and higher switching frequency, will take many hours to do, and if parameters like gate resistance, gate-drive supply and load currents are varied, optimized design is almost impossible. Among the important power electronic devices, the power diode model has been improved in [21] and the IGBT model is developed in [22]. Both component models are based on the SABER simulator. In [23], corresponding models are implemented in SPICE. Practical implementation of a proposed model of a power diode is suggested in [24] using both SPICE and SABER.

The functional definition of a switching converter is used to model three-phase VSI or CSI using PSpice [11]. Simplified device models using controlled sources have been proposed to speed up the simulation. For further simplification, each converter is simulated as a multiport network, wherein the time solution of the currents and voltages, in the input and output terminal, constitute the main objective of the analysis.

A considerable attention has been directed towards enhancing the performance of power converters. Multilevel waveforms are used to reduce the harmonic distortion and increase the power rating of high-performance inverter power supplies [25]. There has been great interest in the neutral point clamped pulse-width modulated (NPC-PWM) inverters drives. The NPC inverter's output voltage may contain fewer

harmonics than that of a conventional full bridge inverter [2] and since the imposed source voltages across the main switching devices are halve the dc source voltage it is particularly attractive in high power applications.

So far, several control schemes for NPC three-level inverters have been proposed. Reported switching pattern based on selective harmonic elimination [2], [26] did not consider the variations of the neutral point potential which is an inherent problem of NPC inverters as pointed out in [27]. Vector control schemes which consider the neutral voltage balance have been reported [28].

The novel rectifier topology examined in this work is an improvement upon the 3-phase Y-switch networks explored in recent articles [29],[30] with the prime application being the input stage to commercial variable speed drives. The converter topologies examined in [29] are essentially SCR harmonic correction units (HCUs) suitable as a retrofit or as a drive option. The work describes a series of techniques using thyristor switches that improve the harmonic content of diode rectifiers connected to a voltage source inverter drive.

A new active interphase reactor for 12-pulse diode rectifier is proposed in [31]. It uses a conventional 12-pulse diode rectifier which requires an interphase reactor to ensure the independent operation of the two parallel-connected three-phase diode bridge rectifiers. In this scheme, a low kVA (0.02 p.u) active current source injects a triangular current into an interphase reactor of a 12-pulse diode rectifier. The proposed system draws near sinusoidal current from the utility with less than 1% THD.

The concept of reducing harmonic distortion associated with rectifier circuits by third harmonic current injection has been reported in [32]-[34]. All the above schemes require a controllable line synchronized external third harmonic current source. Scheme [34] necessitates the use of an input isolation transformer along with the access to its neutral terminal. [32] uses tuned L-C branches in a network that injects total third-harmonic modulated current into the ac terminals of the rectifier. A modification of the scheme uses a magnetic device for current injection in a 3-phase, sinusoidal-current utility interface.

modification of the scheme uses a magnetic device for current injection in a 3-phase, sinusoidal-current utility interface.

1.4 Organization of the Thesis

The thesis begins with an introduction to the SPICE software with emphasis to the latest version of SPICE3. SPICE3 has been very useful for the simulation of power electronic circuits. The introduction of the B-statement and U-statement facilitates the simulation of various complex circuitry. An overview of the SPICE simulator is discussed which is important in solving various problems during simulation.

The rectifier stages of the drive topology are then described. The 6-pulse diode bridge is discussed with emphasis to the performance with a C dc-link filter and LC dc-link filter. Two series connected 6-pulse diode bridge rectifiers give a 12-pulse operation that is very useful for high power applications. The input stage to the 12-pulse rectifier is a Δ-Δ, Δ-Y transformer with their output voltages phase shifted at 30° from each other. The modeling of the Δ-Δ, Δ-Y transformer is done using d-q axis theory. The use of B-statements help to simulate the transformer model very easily by decoupling the input of the rectifier from its output. The comparison of simulation results with experimental ones agree very closely.

The inverter stage can either be a Voltage Source Inverter (VSI) or a Current Source Inverter (CSI) [4], [36]. Both the square wave VSI and the pulsewidth modulated VSI is discussed. The PWM VSI inverter combines both voltage and frequency control within itself and the high switching operation eliminates the voltage harmonics from the output [37]. The inverter leg is modeled using three B-statements that represent the switching function of the six switching devices. A generalized structure of a three-level voltage source inverter is presented with its simulation waveforms. Comparison of the simulated and experimental results for the waveforms and the harmonic analysis of the output voltage are presented for each of the VSI.

The Current Source Inverter is discussed next. A variable dc link voltage is generated by phase control, which is converted to current source by connecting a

series inductance. The CSI is modeled in much the same way as the VSI with three B functions generating the PWM switching pattern. Capacitors are connected at the output of the inverter to absorb high frequency harmonics associated with the PWM inverter output current. The CSI is also viewed with reference to a constant current source inverter where the dc current fed to the inverter is kept constant using a closed loop scheme.

The output stage of the drive is the Induction Motor which is described next. The motor is modeled using d-q axis theory. The elimination of the time-varying components in the d-q axis theory, helps to model the motor easily using voltage functions. The simulation waveforms for the direct-on-line starting of the motor is presented. The operation of the induction motor with constant V/f is explained and various curves are obtained using SPICE3 simulation.

The general features of the variable speed drives with emphasis to the PWM inverter drives summarizes the various stages of the drive topology. A 12-pulse, 3-level PWM voltage source inverter is simulated in one single drive structure to demonstrate the capability and flexibility of SPICE3 for complex circuit simulation.

The thesis concludes by examining a novel rectifier topology that draws a line current with low total harmonic distortion at unity power factor. A resonant network is used to build up a current prior to the natural conduction of the diodes thus helping in waveshaping the line current. SPICE3 simulation waveforms are used to compare with the experimental results. The interactive interpreter, which is a new feature in SPICE3 is used to generate data for the performance analysis of the rectifier topology. The analysis and design of a new rectifier topology with the help of SPICE3 simulation tools is well established.

Chapter 2

INTRODUCTION TO SPICE SIMULATION

Circuit simulation is becoming an indispensable tool for circuit design in power electronic drive systems. Numerical analysis of electrical circuits appeal to the circuit designer as an alternative to tedious hand calculations. This concept facilitates the augmenting or supplanting the laboratory testing in general. This chapter introduces the SPICE3 simulator and explains the various features of circuit simulation tools. The general format of SPICE is described with emphasis to its use in power electronic applications.

2.1 The SPICE Simulator

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general purpose electronic circuit simulation program. Since its introduction, SPICE has gone through its own evolution. The final upgraded version of SPICE is SPICE3 which was converted from the original FORTRAN program to the C program, though the core algorithm have stayed the same. SPICE3f4 is the latest version in the long line of circuit simulators from University of California, Berkeley, which are generally known under the family name of SPICE. It evolved from the older SPICE2g6 and is gradually replacing the latter as the de facto standard among both academic and industrial SPICE simulators.

SPICE falls under the category of continuous time simulator. The time for computer solutions as shown in Fig. 2.1 for such simulators consists of two parts

T_{form} - time to set up the modified nodal admittance matrix

T_{sol} - time to solve the equations

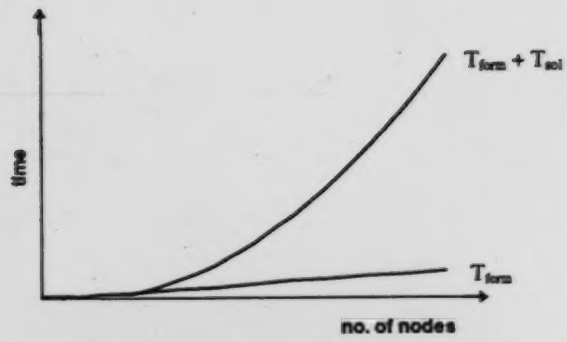


Fig. 2.1 SPICE3 simulator performance curve

The time required to form the matrix is linear with the number of nodes. The time to solve the equations grows as n^3 [38]. In SPICE if a lot of nodes are connected to ground then we get a sparse matrix and a faster solution is obtained using the Sparse Matrix Technique, instead of the usual Gauss Elimination technique. The salient features of the Sparse Matrix Technique are

- Stores only non-zero elements
- Performs operations only on non-zero elements
- Processing order is determined, before the matrix entries are known, to minimize "fill-ins".

With smaller number of nodes, time to form matrix is much greater than the time for the solution. SPICE primarily uses Nodal Analysis for circuit equation formulation.

Nodal Analysis uses the following methodologies for forming the nodal matrix

- Kirchoff's current law (KCL) - this is the starting point
- Kirchoff's voltage law (KVL)

Once the matrix has been formed it proceed to solve the equations thus formed.

For a system of "n" equations,

$$Ax = b$$

the solution methods would be :

Matrix inversion

- Cramer's rule
- $x = A^{-1}b$, n^3 operations for inversion

Gaussian elimination

- forward elimination to form upper triangular system and backward substitution
- $n^3 / 3 + n^3 - n / 3$ operations

LU decomposition

- modified form of Gaussian elimination
- reduction of A into L and U
- forward elimination and backward substitution

It can be seen from Fig. 2.1 , that the matrix solution time is significantly smaller than the device evaluation time, although the difference decreases as the circuit size increases [38].

2.2 Format of circuit files

A circuit file that is read by the SPICE3 simulator is generated by the schematic capture software. The circuit file can be divided into five parts

(1) the title describing the type of circuit or any other comment.

(2) the circuit describing the circuit elements and set of model parameters

(3) the analysis description which defines the type of analysis

(4) the output description which defines the way the output is to be presented

(5) the end of the program

A circuit is described by statements stored in the circuit file. Each statement is self contained and independent of every other statement. Each element in the circuit is connected between nodes that are assigned numbers. Node 0 is predefined as the ground. The first statement of the file is always a comment line. The value of the circuit is written after the nodes to which the element is connected. Models may be used to assign values to the various parameters of the circuit elements. Of the various types of analysis that SPICE offers, the time domain analysis, specified by the .TRAN

statement, is used in the majority of the work. The transient analysis portion of SPICE computes the transients output variables as a function of time over a user-specified time interval. The initial conditions are automatically determined by a dc analysis. All sources which are not time dependent (for example, power supplies) are set to their dc values. The last line of the circuit file terminates with the .END statement.

Given below in Fig. 2.2 is the circuit diagram for a simple half wave diode rectifier and Fig. 2.3, is an example of its SPICE3 schematic with its corresponding circuit file.

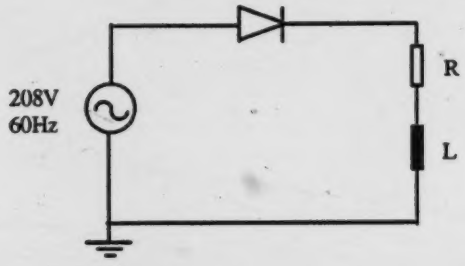


Fig. 2.2 Circuit diagram for Half wave diode rectifier

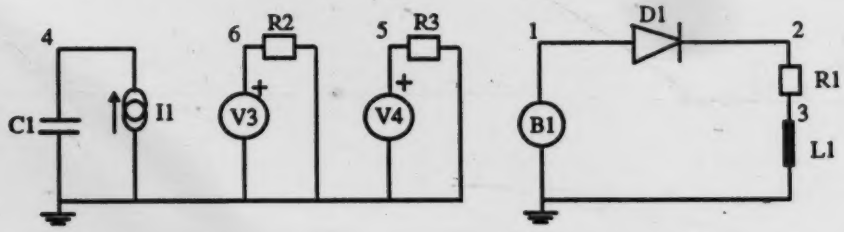


Fig. 2.3 SPICE3 schematic for a half wave diode rectifier

```
*     half wave diode rectifier
.TRAN 20US 116.67MS 100MS 20US UIC
.OPTIONS METHOD=GEAR RELTOL=0.03 ABSTOL=1E-4
.MODEL PD D
R1 2 3 1K
```

```
L1 3 0 2.5MH
B1 1 0 V=V(6)*SIN(V(5)*V(4))    * V = Vm * sin( ω * t )
C1 4 0 1F IC = 0
V3 6 0 DC 294
R2 0 6 1K
I1 0 4 1
V4 5 0 DC 377
R3 0 5 1K
D1 1 2 PD D
.END
```

The input sinusoidal voltage to the rectifier is a B-statement which is made to be a voltage function. The amplitude of the sine function is 294V (208x√2), modeled as a dc voltage source across nodes 6 and 0. Similarly the frequency of the sine wave is modeled as a dc voltage source of magnitude 60V across nodes 5 and 0 corresponding to a 60Hz frequency. The time in SPICE3 is modeled with a constant current source feeding a capacitor. The capacitor charges and ramps up linearly so that the voltage across the capacitor gives the time reference in the simulation. This kind of a model gives circuit functions access to time as a voltage for e.g. a B-statement and can be very useful for PWM circuits with repeated saw tooth functions.

Two types of numerical integration techniques are available in SPICE3f4: the Trapezoidal method and the Gear method. It has been found that using the Gear method for simulating circuits containing power diode model can reduce convergence problems [38].

2.3 SPICE for power electronics circuit simulation

The switching nature of power electronic devices cause the analysis of power electronic circuits to be very difficult. SPICE simulation provides an easy solution to this. The choice of a circuit model depends upon the objective of the simulation. If the goal is to study a circuit to gain an understanding of the principle of operation,

components should be as elementary as possible. Avoiding the use of actual non-linear relationships for the device hastens the speed of simulation.

The major advantage of using SPICE in power electronics is that with the same software a particular circuit can be analyzed and designed at various system and subsystem levels, i.e. at the level of the power switch or the circuit system as a whole [12]. However, for higher levels of simulation, a much simpler model for the devices is chosen for the circuit implementation to minimize convergence problems and reduce the run times.

Power Electronic circuits are frequently coupled to Drive Systems. A variable speed AC machine connected to the rectifier-inverter system gives rise to complex stability problems. The machine is a non-linear multivariable system and interacts dynamically with the source impedance of the drive. Further complexity may arise when for instance multiple machines are fed by a single inverter or multiple rectifiers feed a single inverter. The analysis of such systems is tedious and computer simulation becomes imperative. The study of new control strategies, the effect of harmonics and the variation of system parameters are also facilitated by simulation results.

The recent updates made to SPICE at University of California, Berkley has made obsolete various simulation techniques often used for power electronic systems [9]. The B-statement and the U-statement introduced in the latest version of SPICE3 i.e. Version 3f4, has simplified the structure of control and switching functions used frequently in Power Electronics. The B-statement can be either a current or voltage function and is used to model various complex circuitry without indulging in the micromodeling and the device characteristics of the switching device. This would prevent long simulation run times and convergence problems. The U-statement is simply a comparison statement that has a value of either 1 or 0 according to its argument. Some of the features of SPICE3 used for power electronic simulation are :

- .OPTIONS - Various parameters of the simulations available in SPICE3 can be altered to control the accuracy, speed or default values for some devices. These parameters are changed via the .OPTIONS line. ABSTOL and RELTOL are the

two most common options used. ABSTOL resets the absolute current error tolerance of the program. RELTOL resets the relative error tolerance of the program.

- .TRAN - This dot command performs transient analysis of the circuit. The general form of .TRAN is

  .TRAN *TSTEP TSTOP TSTART TMAX UIC*

  TSTEP is the plotting increment for the output. For use with the post-processor, TSTEP is the suggested computing increment. TSTOP is the final time, and TSTART is the initial time. If TSTART is omitted, it is assumed to be zero. The transient analysis always begins at time zero. TMAX is useful when one wishes to guarantee a computing interval which is smaller than the printer increment, TSTEP. This would also ensure a more accurate numerical integration.

  One of the advantages of choosing a small TSTEP is that it increases the resolution of the waveforms obtained from SPICE3 simulation. This feature is made use of in cases where the experimental waveforms have a resolution that is restricted by the resolution of the oscilloscope. This is frequently seen in the simulation waveform of PWM Inverters where high switching frequency is used.

- .IC - The IC line is for setting the transient initial conditions. When the UIC parameter is specified on the .TRAN line, then the node voltages specified on the .IC control line are used to compute the capacitor, diode and inductor initial condition. Since no dc bias solution is compared before the transient analysis, it is important to specify all dc source voltages on the .IC control line if they are to be used to compute device initial conditions.

- .PRINT - The Print line helps in generating data for the vectors following the print command. Output variables can be specified for any kind of analysis such as TRAN (for transients analysis) just before the list of vectors.

  .PRINT TRAN *vector1 vector2 ...*

- .FOUR - The Four (or Fourier) line controls whether SPICE performs analysis as a part of the transient analysis. The dc component and the first nine harmonics are determined.
- .MODEL - Some devices that are included in SPICE require many parameter values. Often, many devices in a circuit are defined by the same set of device model parameters. For these reasons, a set of device model parameters is defines on a separate .MODEL line and assigned model name. The device element lines in SPICE then refer to the model name.

In addition, SPICE3 is provided with the Interactive Interpreter that helps to monitor parameters in a single run by means of a do loop. The stand alone program is in the form of a .CONTROL file that uses simple syntax similar to C and the shell script. This feature of SPICE3 has been very useful in the performance analysis of Power Electronic circuits. Some of the features of the interactive interpreter are :

- alias : It creates an alias for a command. It can be used to cause a word to be aliased to text.
- alter : It changes a device or model parameter.
- destroy : It releases the memory holding the data for the specified run.
- echo : It prints out the given text to the screen during the simulation run.
- print : It prints the vectors described by the expression following the print statement. If the col argument is present, it prints the vectors named side by side in column format. If the line argument is given, the vectors are printed horizontally.

2.4 Troubleshooting

The major reason for any SPICE3 simulation to abort is due to convergence problems. Both the DC and transient solutions are obtained by an iterative process which is terminated when both of the following conditions hold:

1) the non-linear branch currents converge to within a tolerance of 0.1% or 1 picoamps, whichever is larger.

2) The node voltages converge to within a tolerance of 0.1% or 1 microvolts, whichever is larger.

The most common reason for failure to converge is simply due to error in specifying circuit connections, element values or model parameters. One characteristic that has been blamed for many SPICE convergence problem is the "floating nodes". These are circuits which have no conductance from the node to any other part of the circuit. This produces a row and column of zeros in the modified nodal analysis matrix, making it impossible to invert in practice.

Another common error is "time step too small". SPICE3 provides an iteration-count system of timestep control. If convergence is not obtained within a maximum number of iterations, the solution is abandoned, the timestep cut by a factor of eight, and the new smaller step is attempted. If the convergence is obtained in fewer than a minimum number of iterations, the timepoint is accepted and the timestep may be doubled before attempting the next step. This technique relies very heavily on a good choice of the starting timestep by the user. To circumvent this error the .TRAN values are redefined, to change the time step for transient analysis. Also the RELTOL and ABSTOL values are changed to resume simulation.

SPICE also runs into convergence problems if in the circuit a capacitor is connected across a voltage source or a current source feeds an inductor. The simulation in this case aborts with an error message "check node #". One way to solve this problem is to add a small resistor to the circuit elements which causes the convergence problem.

Chapter 3

DIODE BRIDGE RECTIFIERS

In most power electronic applications, the power input is in the form of a 50 or 60 Hz sinewave ac voltage provided by the electric utility, which is first converted to a dc voltage. A majority of the power electronic applications such as switching dc power supplies, ac-motor drives and so on, use uncontrolled rectifiers. This chapter discusses the six-pulse and twelve-pulse diode bridge rectifier topologies. A model for the Δ-Δ, Δ-Y transformer is presented using d-q axis theory. Simulated and experimental results are presented for comparison. The simulated and experimental performance analysis of the rectifier is done with emphasis on the line current harmonics and the THD.

3.1 Six-Pulse Diode Bridge Rectifier

In industrial applications where three-phase ac voltages are available, it is preferable to use three phase rectifier circuits as compared to single-phase rectifiers. Three-phase rectifiers have lower ripple content in the waveforms and a higher power handling capability. A simple circuit for a six-pulse diode bridge rectifier with LC dc-link filter is shown in Fig. 3.1.

The input line current of the three phase rectifier deviates from being perfectly sinusoidal. By Fourier Analysis, the line current can be expressed in terms of the fundamental frequency and other harmonic components. If the line voltage is assumed to be purely sinusoidal, then only the fundamental component of the line current contributes to the average power flow. The line current harmonics are generally dominated by odd harmonics.

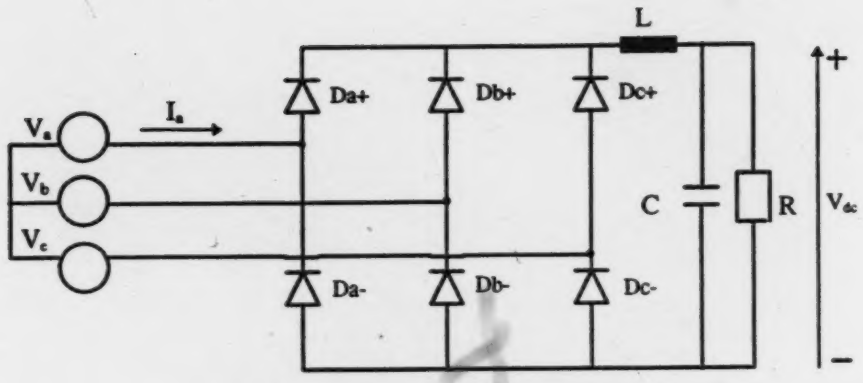


Fig. 3.1 Three-phase diode bridge rectifier circuit

For a three phase diode bridge rectifier with an LC dc-link filter, see Fig. 3.1 the line current harmonics (assuming L -> ∞) are theoretically given as :

$$I_a = \frac{2\sqrt{3}}{\pi} I_o \left(\sin\theta - \frac{1}{5}\sin 5\theta + \frac{1}{7}\sin 7\theta - \frac{1}{11}\sin 11\theta + \frac{1}{13}\sin 13\theta \ldots\ldots\right) \qquad (3.1)$$

In a diode bridge rectifier, two devices conduct at any instant. Each diode conducts for 120° per cycle and a new diode begins to conduct after a 60° interval. The output rectified waveform which consists of portions of the line-to-line current ac voltage waveforms, repeat with a 60° duration, making this a six-pulse rectifier.

3.1.1 Simulation of 6-pulse diode bridge rectifier

SPICE3 simulation and modeling is performed for a better understanding of the analysis of the bridge rectifier. Broadly there are two approaches in modeling the behavior of a semiconductor device like a diode. A macro-model, mainly based on an empirical approach, is one that does not take into account the geometry and the physical process of the device. This is to be distinguished from a micro-model that is based on the physical phenomena within the semiconductor model. In the present

work, we use a SPICE model of the diode such that the device's known input/output behavior is presented by an electrical equivalent circuit [25] and can be expressed in terms of its model parameter like breakdown voltage(BV), junction capacitance (CJO) and inverse saturation current (IS). Model parameters for the diode are defined on a separate .MODEL line. The SPICE library has a model for power diode which is aliased as "PD" (power diode) and is used for the present circuit.

3.1.2 C dc-link filter

The SPICE3 model for the 3-phase diode bridge is shown in Fig. 3.2. In this rectifier topology we have a large C (940μF) dc-link filter at the rectifier output. For all practical applications a finite source inductance is always present. The values of the output capacitor and load are exactly the same as used in the experimental setup. The

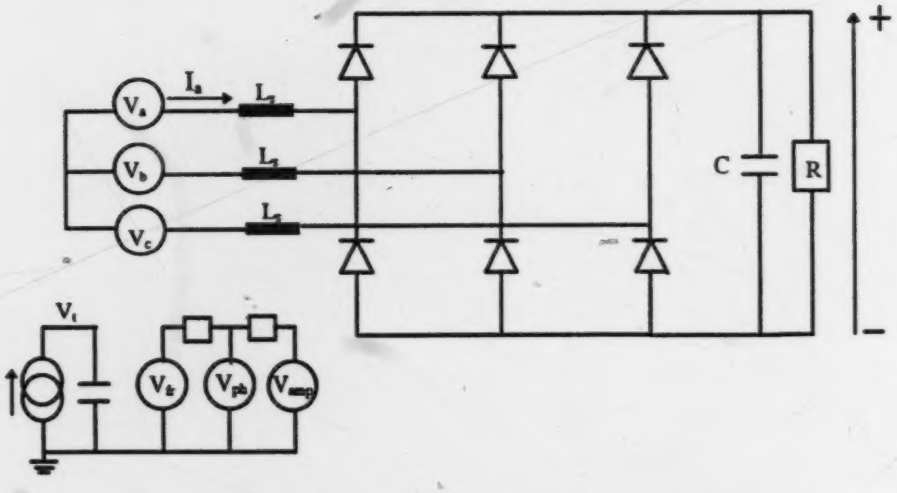


Fig. 3.2 SPICE3 model for 6-pulse rectifier bridge with C filter

input source inductance in the power electronics laboratory was estimated to be about 0.4 mH. The effect of the line inductance is to slope off the vertical portion on the line current. This attenuates the higher order harmonics in particular. The SPICE3

schematic and its corresponding netlist for the six-pulse diode bridge rectifier is given in Appendix G.1. The salient features of the SPICE model in Fig. 3.2 are :

- input sinusoidal voltage, V_a

  $V_a = V_{amp} * \sin(V_{fr} * V_t + V_{ph})$

  The input sinusoidal voltage is modeled with the help of a B-statement which is a voltage function representing the sinusoidal.

- time, V_t :

  The time is modeled as the constant current source in parallel with a capacitor. The capacitor charges and ramps up linearly, thus the voltage node represents time.

- amplitude, V_{amp} :

  The amplitude of the sinusoidal wave is modeled as a constant dc voltage source of magnitude 169V ($\sqrt{2}$ x 208 /$\sqrt{3}$).

- frequency, V_{fr} :

  The frequency of the sinusoidal wave is modeled as a constant dc voltage source of magnitude 60V corresponding to 60Hz.

- phase, V_{ph} :

  The phase shift between the three phase voltages of the sinusoidal wave is modeled as a constant dc voltage source of magnitude 120V which corresponds to 120°.

3.1.3 Waveforms and analysis for C filter

The simulated and experimental waveforms are shown in Fig. 3.3. As seen from Fig. 3.3(a),(b) the output current is always discontinuous. This is more prominent in the experimental waveform of the current. The reason being that the source inductance for the simulation could not be lowered below 0.4mH. With a voltage function feeding an inductor, any attempt to lower the inductance value causes a convergence problem, a problem commonly encountered in SPICE3. A larger value of source inductance in the simulation also causes larger commutation overlap as seen in Fig. 3.3 (a). Two current pulses are drawn from each phase during every half-cycle.

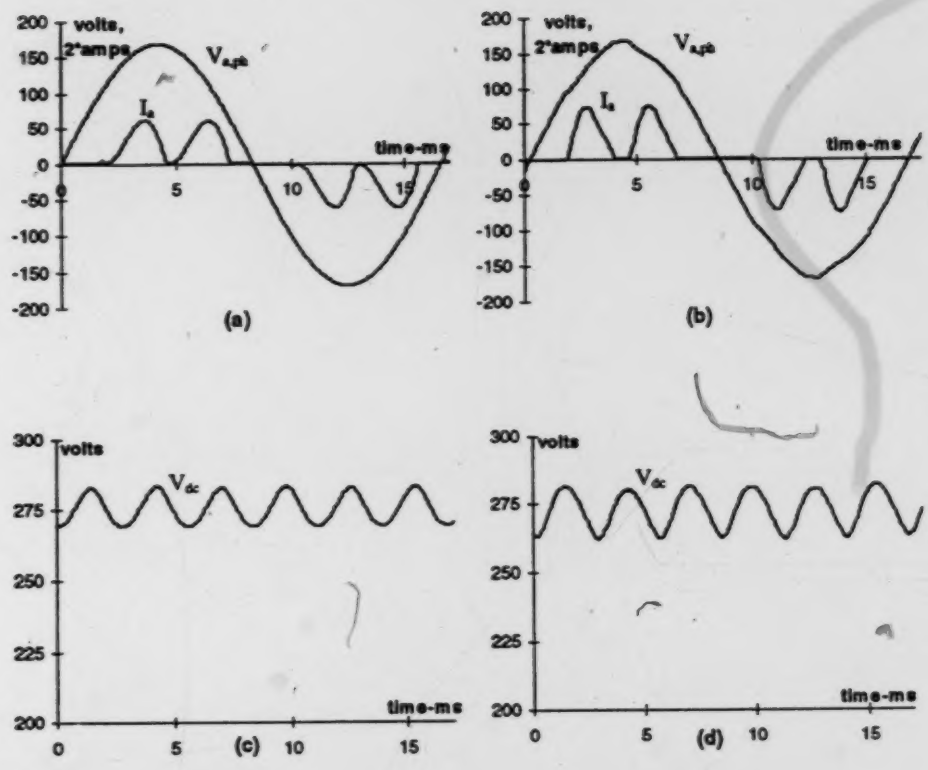


Fig. 3.3 Simulated and experimental waveforms for 6-pulse rectifier with C-filter, (a) simulated phase voltage and line current, (b) experimental phase voltage and line current, (c) simulated 6-pulse output rectified voltage, (d) experimental 6-pulse output rectified voltage.

3.1.4 Harmonic analysis for C-filter

Harmonic analysis and the various performance analysis through both experimental data and SPICE3 simulation is given in the Appendix A. Large values of THD are obtained because of dominant 5^{th} and 7^{th} harmonics. A lower value of THD of 68.3 % is obtained by simulation as compared to the experimental THD of 84.4 % because we used a larger source inductance in the simulation. A larger source inductance also results in a better PF of 0.81 as compared to the experimental PF of 0.77.

3.1.5 LC dc-link filter

Often in three-phase rectifiers, an inductor placed on the dc side between the rectifier and the filter capacitor is used to improve the current waveforms and the ripple in the dc voltage output. It is possible to calculate the minimum value of inductance required to make the output current continuous for a given value of output current and input line-to-line voltage as follows :

$$L_{d\,min} = \frac{0.013\ V_{11}}{\omega I_o} \qquad (3.2)$$

Assuming the source inductance to be zero, an increase in the dc-side inductance improves the input power factor and if it is made large enough, such that the output current becomes essentially constant and ripple free, the PF approaches 0.955. Also at light loads the output current tends to be discontinuous. The order and magnitude of the theoretical current harmonics for a 6-pulse converter with LC filter can be determined from

$$\frac{I_h}{I_1} = \frac{1}{h} \qquad (3.3)$$

where $h = 6k \pm 1$, $k = 1, 2, 3.....$

3.1.6 Waveforms and analysis for LC-filter

Fig. 3.4 shows the simulated and experimental waveforms of the 6-pulse rectifier with LC dc-link filter. The presence of an inductor in the dc-link causes the current to be continuous as seen from Fig. 3.4(a),(b). The output rectified voltage is substantially lower as compared with the no-inductance case. The L and the C together form a low pass filter and, therefore, the peak-to-peak ripple in the rectified output voltage is less. The overall efficiency remains essentially the same as that with a C-filter; there are additional losses in the inductor, but the conduction losses in the diodes are lower.

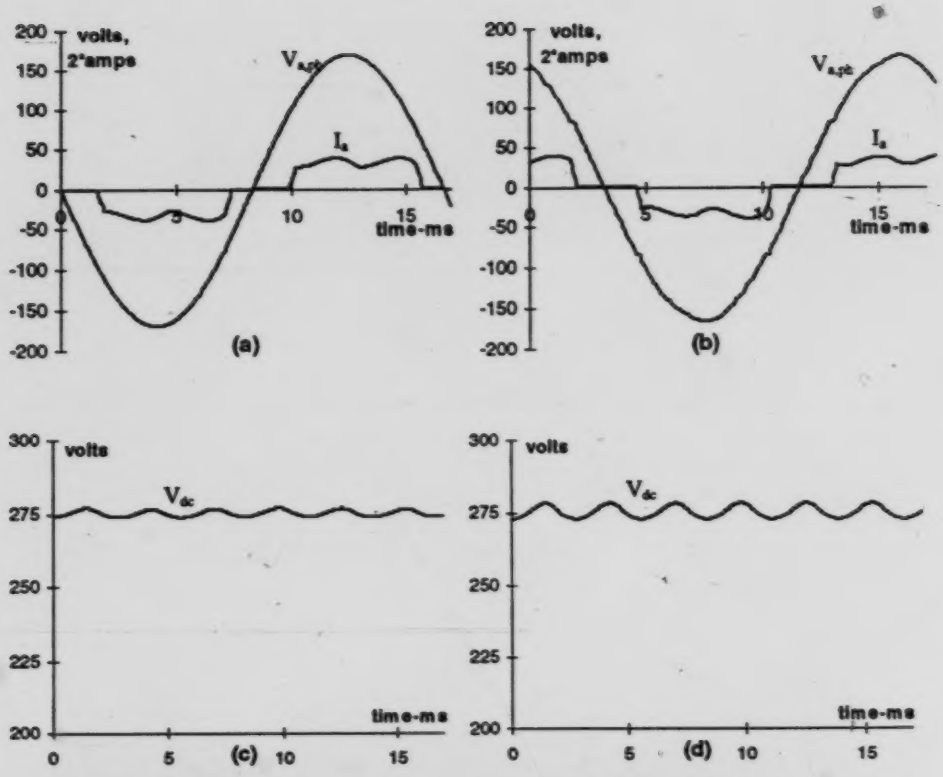


Fig. 3.4 Simulated and experimental waveforms for 6-pulse rectifier with LC-filter, (a) simulated phase voltage and line current, (b) experimental phase voltage and line current, (c) simulated 6-pulse output rectified voltage, (d) experimental 6-pulse output rectified voltage.

3.1.7 Harmonic analysis for LC-filter

Harmonic analysis and the various performance analysis through both experimental data and SPICE3 simulation is given in Appendix A. The 5th and the 7th line current harmonics are drastically reduced on addition of the inductor in the dc-link, as compared to the case with only a C-filter. This results in a low THD of 27.6%. The THD obtained by simulation is better than the theoretical THD of 31%, because of a finite source inductance that improves the PF and hence results in a better THD.

The assumption of 1/h per unit harmonics, even when modified to allow for the attenuating effects of the commutation, do not adequately describe the actual magnitude of 6-pulse converter harmonic currents in many cases. To accurately

determine the characteristic converter harmonics, a calculation procedure which takes into account the ripple of the dc current reflected back into the ac line current must be performed [6]. Evaluation of these ripple effects will tend to increase the magnitude of the 5th harmonic while decreasing the magnitude of the higher order characteristic harmonics.

3.2 Twelve-Pulse Diode Bridge Rectifier

For higher power applications, when the converter current or voltage is high, diode bridges may be connected in series or parallel. For the present work, the series connection of two diode bridges on the dc side is used. One converter bridge is fed from a Δ-Y transformer that introduces a three phase set of secondary voltages shifted by 30° with respect to the primary voltage. The other converter bridge is fed by a secondary voltage, from a Δ-Δ transformer, which has no phase shift. Due to the phase relationships it is seen that some of the current harmonics in one bridge are in antiphase with those of the other. Thus, these phase shifting transformers provide mechanism for harmonic cancellation. In addition, they reduce the dc voltage output

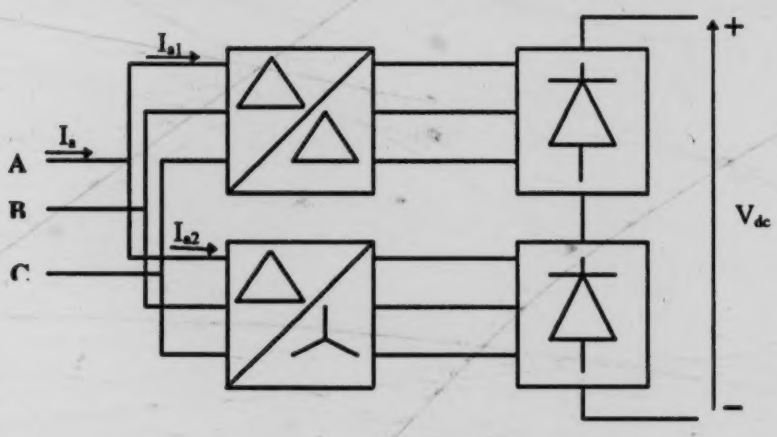


Fig. 3.5 Block Diagram for 12-pulse diode bridge rectifier

ripple. This effectively reduces the size of the filter used in the dc-link. Operation with increasing pulse number is very desirable for high-power converter applications such as HVDC and large dc motor drives [39].

The harmonic cancellation of the input line current in terms of the Fourier components is

$$I_{a1} = \frac{\sqrt{3}}{N\pi} I_o \left(\cos\theta - \frac{1}{5}\cos 5\theta + \frac{1}{7}\cos 7\theta - \frac{1}{11}\cos 11\theta + \frac{1}{13}\cos 13\theta \ldots\right) \quad (3.4)$$

$$I_{a2} = \frac{\sqrt{3}}{N\pi} I_o \left(\cos\theta + \frac{1}{5}\cos 5\theta - \frac{1}{7}\cos 7\theta - \frac{1}{11}\cos 11\theta + \frac{1}{13}\cos 13\theta \ldots\right) \quad (3.5)$$

$$I_a = I_{a1} + I_{a2} = \frac{2\sqrt{3}}{N\pi} I_o \left(\cos\theta - \frac{1}{11}\cos 11\theta + \frac{1}{13}\cos 13\theta \ldots\right) \quad (3.6)$$

In the operation of such multipulse converters, it is assumed that the dc circuit is filtered such that any ripple caused by the dc load does not significantly affect the dc current. This is true for passive loads and for most converters feeding dc power to voltage source inverters. It is less likely to be true for inverter loads of the current source type, where practical filtering may be insufficient to prevent dc load ripple from effecting the total ripple.

3.2.1 d-q Axis Theory model for Δ-Δ/Δ-Y transformer

The input of the 12-pulse rectifier bridge is the Δ-Δ/Δ-Y transformer, with their secondaries phase shifted by 30°. The series impedance of the autotransformer used in the experimental setup is taken into account in the simulation by using higher inductance values for the Δ-Δ/Δ-Y transformer.

The equivalent per phase circuit of the transformer is considered in terms of the d-q axis theory [40]. In this theory the time varying parameters are eliminated and the variables and parameters are expressed in orthogonal or mutually decoupled direct (d) and quadrature (q) axes, see Fig. 3.6. The supply voltages in terms of d and q voltages are written in matrix form as

$$\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta & 1 \\ \sin(\theta+120) & \cos(\theta+120) & 1 \\ \sin(\theta-120) & \cos(\theta-120) & 1 \end{bmatrix} \bullet \begin{bmatrix} Vq \\ Vd \\ Vo \end{bmatrix} \qquad (3.7)$$

where V_o is the zero sequence component which does not exist for a balanced three-phase condition. The angle θ is arbitrary between the two sets of axes.

Setting $\theta = 0$, the d-axis will coincide with V_a and ignoring the zero sequence component, the above matrix equation yields the following transformation relations:

$$V_d = (2V_a - V_b - V_c) / 3 \qquad (3.8)$$

$$V_q = (V_b - V_c) / \sqrt{3} \qquad (3.9)$$

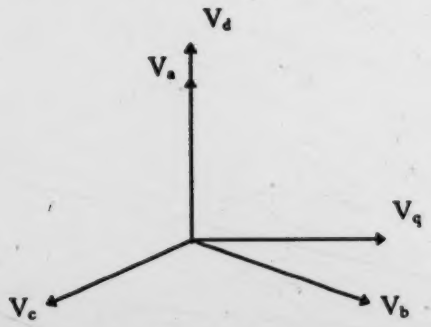


Fig. 3.6 Phasor diagram for d-q transformation for Δ-Δ transformer

3.2.2 SPICE3 model for Δ-Δ/Δ-Y transformer

The Δ-Δ /Δ-Y transformer is modeled by considering two separate d-q per phase equivalent circuits having identical parameters. The parameter values for simulation are the same as the one used in the experimental setup. The data for the various tests - Open Circuit Test and Short Circuit Test done on the Δ-Δ /Δ-Y transformer is given in Appendix B. Each phase is supplied with the V_d and V_q voltages by means of voltage functions using B-statements. The SPICE3 schematic with its corresponding netlist is given in Appendix G.2. The current flowing in the respective primaries are reflected back to the supply side. Similarly the secondary

currents are reflected into the load side. The expression for the phase currents in terms of the d and q currents flowing in the Δ-Δ transformer is

$$I_{a1} = I_d \tag{3.10}$$

$$I_{b1} = -\frac{1}{2} I_d + \frac{\sqrt{3}}{2} I_q \tag{3.11}$$

$$I_{c1} = -\frac{1}{2} I_d + \frac{\sqrt{3}}{2} I_q \tag{3.12}$$

The Δ-Y model differs from the Δ-Δ model in that its input supply voltage is 30° phase shifted. The phasor diagram for the Δ-Y secondary phase voltages in terms of the d and q voltages is given in Fig. 3.7

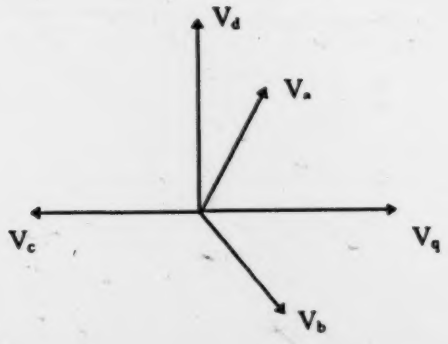


Fig. 3.7 Phasor diagram for d-q transformation of the Δ-Y transformer

Similarly, the d and q voltages fed to the Δ-Y per phase equivalent circuit is given by the transformation

$$V_d = -(2V_c - V_a - V_b) / 3 \tag{3.13}$$

$$V_q = (V_a - V_b) / \sqrt{3} \tag{3.14}$$

and the current relationships are

$$I_{a2} = \frac{\sqrt{3}}{2} V_d + \frac{1}{2} V_q \tag{3.15}$$

$$I_{b2} = -\frac{\sqrt{3}}{2} V_d + \frac{1}{2} V_q \tag{3.16}$$

$$I_{c2} = - V_q \tag{3.17}$$

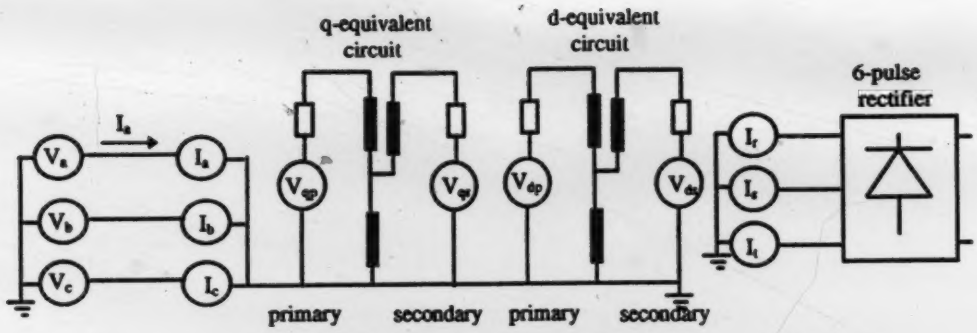


Fig. 3.8 d-q axis theory transformer model

The SPICE model for the Δ-Δ transformer is shown in Fig. 3.8 and is obtained from the various equations derived from the d-q axis theory. Each transformer model consists of separate d and q equivalent circuits with a primary and a secondary. The input to the transformer is the three phase voltages V_a, V_b, V_c with phase a represented by a B-statement which is voltage function as explained in section 3.1.2.

Each of the primaries are fed by a B-statement which is a voltage function and is a functional relationship of the input phase voltages. These voltage relations are obtained from Equations (3.8),(3.9).

d-equivalent circuit primary: $V_{dp} = (2*V_a-V_b-V_c) / 3$ (3.18)

q-equivalent circuit primary: $V_{qp} = (V_b-V_c) / \sqrt{3}$ (3.19)

The currents flowing in the primaries of each of the equivalent circuit is reflected back to the input side with the help of B-statements that are functions of the current flowing through the B-statements in the two primaries. These current relations are obtained from Equations (3.10), (3.11), (3.12).

Phase a : $I_a = I(V_{dp})$ (3.20)

Phase b : $I_b = 0.5*(-I(V_{dp})+1.732*I(V_{qp}))$ (3.21)

Phase c : $I_c = -0.5*(I(V_{dp})+1.732*I(V_{qp}))$ (3.22)

where V_{dp} and V_{qp} are the voltage functions in the primary side of the d and q equivalent circuit respectively.

Similarly, the secondaries of the d and q equivalent circuits are fed by a B function which is a voltage functions of the output voltages. The current in the secondaries are reflected to the output and are functions of the current flowing through the B-statements in the two secondaries. The three output B-statements thus function as the input voltage to the 6-pulse diode bridge rectifier.

3.2.3 SPICE3 model for 12-pulse rectifier

The SPICE3 model of the 12-pulse diode bridge rectifier is shown in Fig. 3.9. Two 6-pulse diode bridges are connected in series to give a 12-pulse operation. The Δ-Δ /Δ-Y transformer has two primaries and two secondaries. The d-q axis voltages and current for the Δ-Δ transformer are defined by Equations (3.8)-(3.12) and the corresponding relationships for the Δ-Y transformer, whose output voltage is 30° phase shifted from the Δ-Δ transformer, are defined by Equations (3.13)-(3.17).

The use of B-statements to decouple the input and the output of the Δ-Δ /Δ-Y transformer helps to simplify the model by avoiding the non-linear interaction between the input and the output. This decoupling leads to more nodes being connected to the ground thus generating a much sparse nodal admittance matrix during simulation. The Sparse Matrix technique thus used increases the speed of simulation.

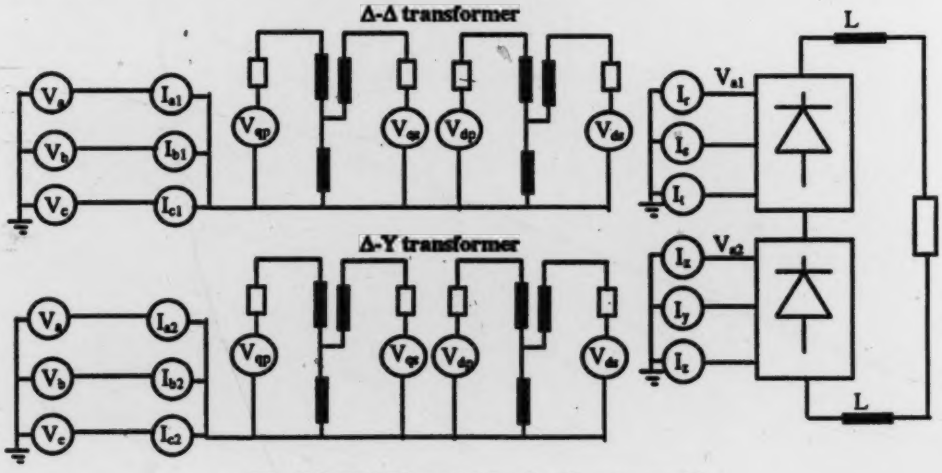


Fig. 3.9 SPICE3 model for the 12-pulse rectifier

3.2.4 Waveforms and analysis for 12-pulse rectifier

Fig. 3.10 shows the simulated line-to-line output voltage and experimental phase voltage waveforms for the Δ-Δ transformer and Δ-Y transformer. Significant commutation overlap is seen in the simulation results due to the large leakage reactance of the transformer. Also, an autotransformer was used in the experimental setup, that further adds to the line inductance. The presence of line inductance does not change the order of characteristic harmonics produced either on the ac side or on the dc side.

Line notching results as shown in Fig. 3.10 due to changeover of current conduction from one device to the other. With diode operation, the current changes naturally from one device to the other, and the notch has one fast rising side. On the other hand with an SCR bridge, the notch will have two fast changing sides, which gives a greater likelihood of high frequency interference. When the converter is operated from the line without phase shift, the line voltage shows one large notch and two smaller notches. On the other hand, if the converter is operated from a phase-shifting transformer, the pattern of notching changes. In the case of the Δ-Y transformer with 30° phase shift, there will be two larger notches. In a 12-pulse circuit formed from two 6-pulse circuits, the load current being commutated is reduced to one-half. Notch area is thus reduced by a factor of 2 for a 12-pulse rectifier as compared to the 6-pulse operation [41].

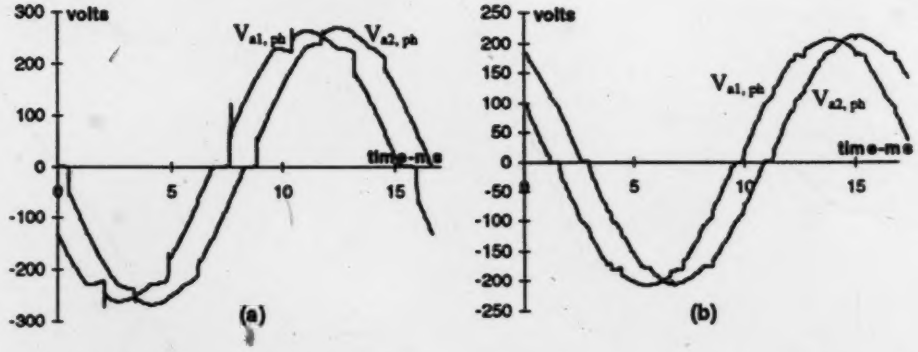


Fig. 3.10 Waveforms for Δ-Δ / Δ-Y transformer, (a) simulated line-to-line output voltage, (b) experimental phase voltage.

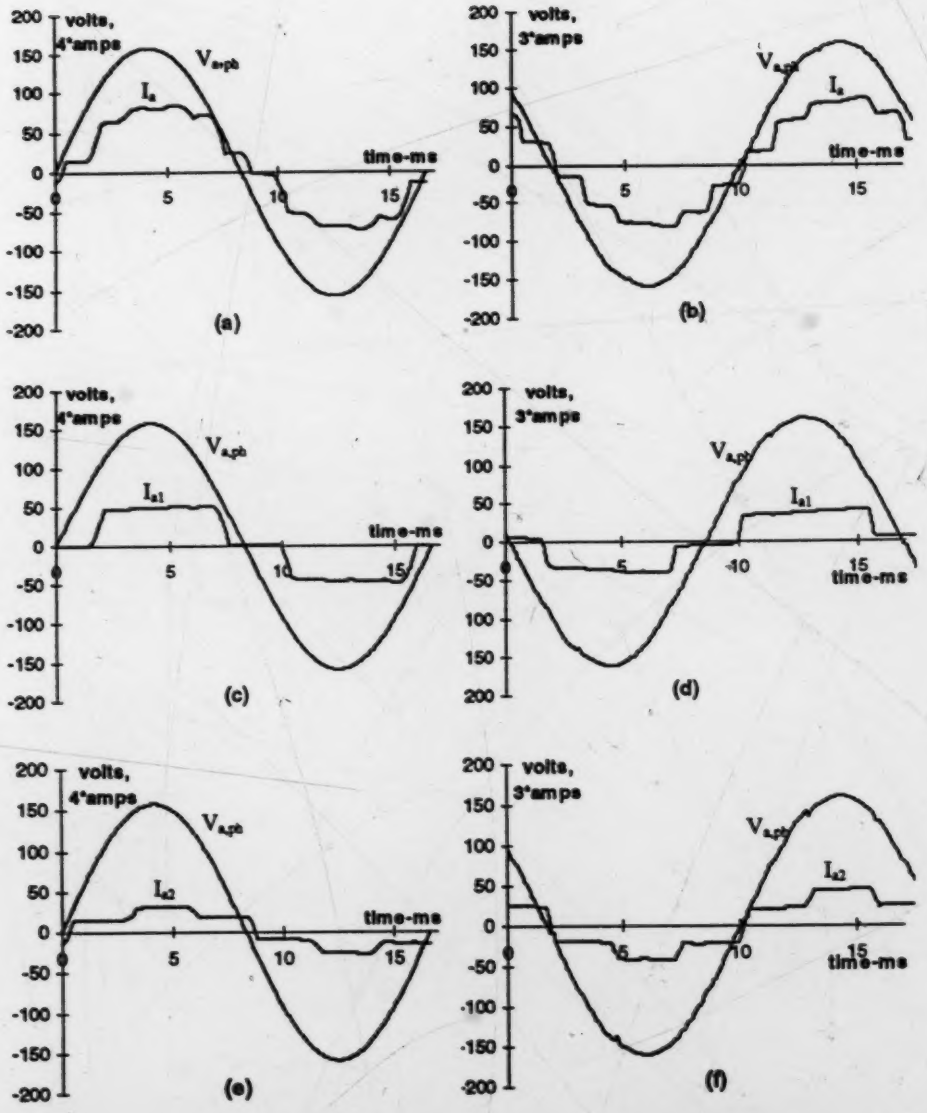


Fig. 3.11 Simulated and experimental line current waveforms for the Δ-Δ/ Δ-Y transformer, (a) simulated phase voltage ($V_{a,ph}$) and total line current , (b) experimental phase voltage and total line current, (c) simulated phase voltage and input line current for the Δ-Δ transformer, (d) experimental phase voltage and input line current for the Δ-Δ transformer, (e) simulated phase voltage and input line current for the Δ-Y transformer, (f) experimental phase voltage and input line current for the Δ-Y transformer.

The 12-pulse rectifier model has two six-pulse diode bridge rectifier connected in series. The load is resistive with a 2.5mH inductor in both the positive and the negative dc rail. The value of the load resistance is the same as used in the experimental setup. Typical waveforms of the different line currents are given in Fig. 3.11. The waveforms are rounded instead of being the theoretical stair-type of waveforms because of the inductive source and leakage impedances.

All the line currents in Fig. 3.11 show significant commutation overlap, which is even more prominent in the simulation due to higher value of leakage reactances used to compensate for the autotransformer used in the experimental setup.

3.2.5 Harmonic analysis for 12-pulse rectifier

Harmonic analysis and the various performance analysis through both experimental data and SPICE3 simulation is given in the Appendix C. The 5^{th} and the 7^{th} line current harmonics theoretically get canceled as suggested by equation (3.4),(3.5) and (3.6). Their negligible small value as seen from Appendix C is due to a slight voltage imbalance of the output of the Δ-Δ transformer and Δ-Y transformer. This results is a low THD of 7.32 %. The experimental THD obtained is 10.9 %. The 12-pulse rectifier has the 11^{th}, 13^{th}, 23^{rd} and other higher order harmonics in the input line current which make filtering relatively easy as compared to 6-pulse operation.

In high power rectifier circuits, the ac line current during output short circuit is sometimes limited by purposely designing a transformer with a high reactance or externally adding a current limiting reactance. This extra reactance with a 12-pulse rectifier circuit drastically reduces the 11^{th} and the 13^{th} harmonic currents of the 60Hz ac system [7].

The output rectified voltage waveforms of the two diode bridges are shown in Fig. 3.12. High dc-link voltage with low voltage ripple is desirable since it reduces the size of the filter. These two 6-pulse waveforms are shifted by 30° with respect to each other. Since these two bridges are connected in series on the dc side the total dc

voltage, V_{dc} has 12 ripple pulses per fundamental ac cycle. This results in the voltage harmonics of the order h in V_{dc}, where

$$h = 12k \quad (k = \text{integer})$$

and the 12th harmonic is the lowest order harmonic.

The six pulses generated by each of the transformer are not identical due to a slight voltage imbalance at the output of the Δ-Δ and Δ-Y transformer. This is due to the fact that, for the Δ-Y transformer the turns ratio of √3 i.e 1.732 is practically very difficult to achieve with a lot of precision.

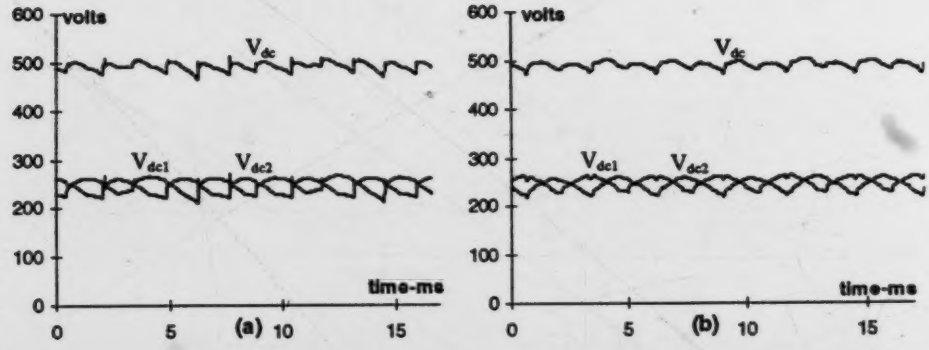


Fig. 3.12 Simulated and experimental output voltage waveforms for the 12-pulse rectifier, (a) simulated 6-pulse and 12-pulse rectified voltage, (b) experimental 6-pulse and 12-pulse rectified voltage.

In order to design more realistic 12-pulse diode bridge rectifier systems, particular attention needs to be given to the voltage distortion already present in the electric utilities due to other nonlinear loads and harmonic resonance conditions. In many industrial systems with nonlinear loads, its is not uncommon to measure 1% to 3% voltage unbalance and/or 2.5% to 5% pre-existing 5th and 7th harmonic voltage distortion when a large percentage of loads are nonlinear [42].

Chapter 4

VOLTAGE SOURCE INVERTER

Inverters convert dc to variable frequency ac. An inverter is categorized as voltage source if, viewed from the load side, the ac terminals of the inverter function as a voltage source. The voltage source inverter can be a square wave inverter or the Pulse Width Modulation (PWM) inverter. In this chapter the SPICE3 simulation of six-pulse, two level square wave inverter and PWM inverter have been discussed. The square wave inverter is modeled using thyristor as the switching device, two in each inverter leg. For the PWM inverter where the switching frequency is much higher, voltage functions are used in each inverter leg instead to facilitate SPICE3 simulation. The experimental and simulated waveforms have been compared. A generalized structure of a three-level, twelve pulse voltage source inverter is also explained along with its SPICE3 simulation. A comparison of the voltage harmonics present in the output have been done using both simulation and experimental data.

4.1 6-pulse, 2-level Square Wave Inverter

The input dc voltage of a square wave voltage source inverter in controlled in order to control the magnitude of the output ac voltage, and therefore the inverter has to control only the frequency of the output voltage. The output ac voltage waveform is similar to a square wave and hence the name.

Each control signal for the six switches in the inverter legs, see Fig. 4.1 has a duration of π radians. The control signals are applied to the switches with a phase difference of $\pi/3$ radians, see Fig. 4.2. The switches in the same leg conduct alternately. Some time must elapse between the turn-off of one switch and turn-on of another switch in the same leg to ensure that the two do not conduct simultaneously and cause a short circuit.

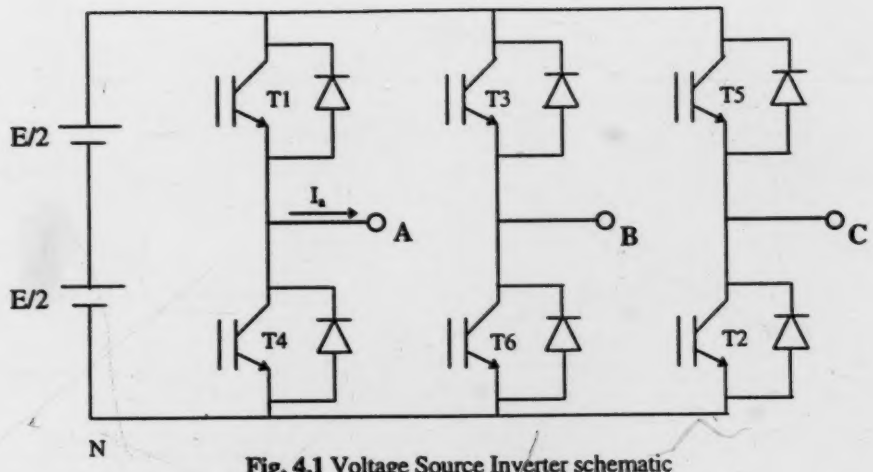


Fig. 4.1 Voltage Source Inverter schematic

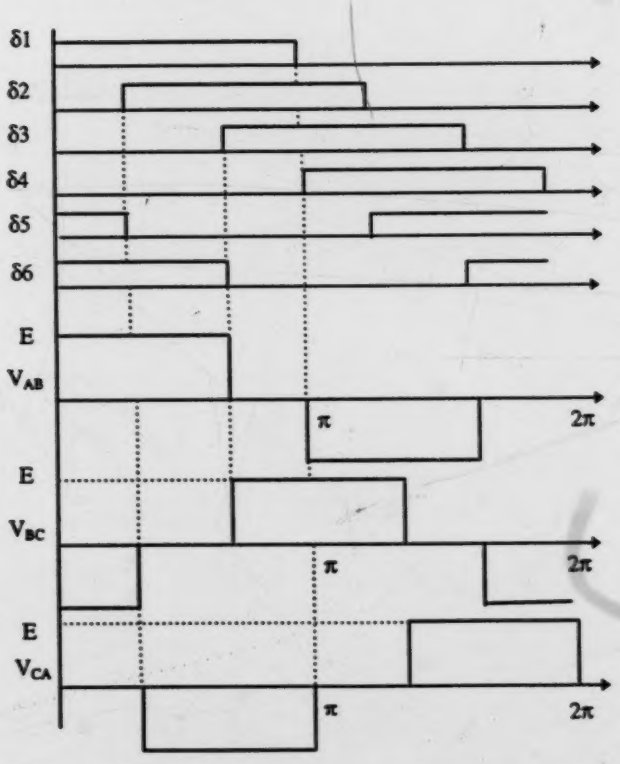


Fig. 4.2 Gating signals and output voltage waveforms for Square Wave VSI

The magnitude of the fundamental frequency line-to-line rms voltage in the output can be obtained from

$$V_{LL1} = \frac{\sqrt{6}}{\pi} E = 0.78\,E \qquad (4.1)$$

The line-to-line output voltage waveform does not depend on the load and contains harmonics ($6n \pm 1$; $n = 1,2,3...$), whose amplitudes decrease inversely proportional to their harmonic order,

$$V_{LLh} = \frac{0.78}{h} E \qquad \text{where } h = 6n \pm 1;\ n = 1,2,3..... \qquad (4.2)$$

4.1.1 SPICE3 simulation of square wave inverter

The circuit for the square wave voltage source inverter is modeled with six switching devices, two in each of the inverter legs. The control signal to the switching devices are generated by voltage functions using B-statements and U-statements and are phase delayed by 60 degrees from each other. The SPICE3 model for the square wave inverter is given in Fig. 4.2. The SPICE3 schematic and the corresponding netlist is given in Appendix G.3.

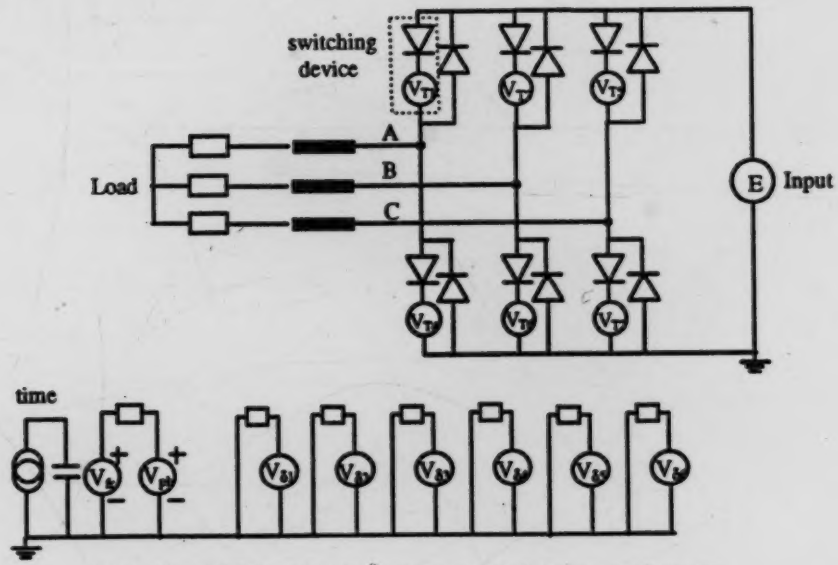


Fig. 4.2 SPICE3 model for square wave voltage source inverter

Each switching device in the inverter leg is fired at intervals of 60°. The 60° delay of the device is modeled with a constant dc voltage source, V_{ph} of magnitude 60V. The conduction period of the six devices are defined by each of the voltage functions $V_{\delta 1}$-$V_{\delta 6}$. $V_{\delta 2}$ for instance would be defined as

$$V_{\delta 2} = U(\text{asin}(\sin(V_{fr}*\text{time} + 1*V_{ph}))) \quad (4.3)$$

The "asin" function converts the sine wave to a triangular sine wave. The U-statement has a value 1 for the period its argument remains greater then zero and has a value of 0 otherwise.

The early device models used in SPICE program represented switching devices, an SCR for instance, by the two complementary bipolar transistor configuration [40]. Giacoletto [10] used the ideal voltage switch provided in PSpice to develop a simple SCR model. One major drawback of this model is that the SCR model is presented as a subcircuit with voltage controlled switch and SPICE takes a long time to solve the admittance matrix for voltage controlled switches where the resistance of the switch changes from a few ohms to some megaohms. The use of six such switching devices in a simple 6-pulse phase controlled rectifier would thus take a considerable amount of simulation time. The switching device used in the model in Fig. 4.2 can be considered as a GTO thyristor.

The above problem is overcome by the provision of a voltage function in SPICE3. The switching device in the above circuit is modeled by having a diode in series with a voltage function using a B-statement as shown in Fig.4.2. The diode maintains the unidirectional property of the device. The voltage function in the device model defines the conduction period. The voltage function is defined as

$$V_{T2} = I_{T2} * (V_{\delta 2}*0.05 + (1- V_{\delta 2})*1e6) \quad (4.4)$$

The device is on as long as a current, I_{T1} flows through it. It is modeled such that the device has a low on state drop and a high reverse biased voltage across it.

For the specified output kVA requirement, a suitable power switching device is to be selected and its output voltage and current ratings have to be designed. The devices have to withstand the maximum input voltage in the forward direction on

which the margin due to commutation overshoot, typically 50% overvoltage, is added. The diodes are usually of the fast-recovery type and have the same voltage rating as the thyristor.

For the purpose of modeling, the input to the voltage source inverter is taken as a rectified dc voltage of the same magnitude as the experimental setup. The rectified voltage can be obtained by employing a controlled rectifier. But this causes large magnitude of low frequency harmonics in the rectifier output voltage and source current resulting in low power factor of the rectifier at low output voltage. Rectified output voltage can also be obtained using a diode bridge rectifier followed by a chopper, such that the power factor remains close to unity under all conditions of operation. The bypass diodes of the inverter clamps the load voltage to the input level and also permit reverse current flow during reactive power flow and regeneration.

The output of the circuit in Fig. 4.2 is star connected to model the induction motor stator. The values for the output used for simulation are the same as the machine parameters for the experimental setup. The tests used to determine the values of the parameters are given in Appendix D.

4.1.2 Waveform and analysis for square wave inverter

The simulated and experimental waveforms are shown in Fig. 4.4. The output line voltage wave waveform, Fig. 4.4 (a),(b) have a characteristic six-stepped wave shape. The line current wave shape is due to the switching action of the devices in the inverter legs. For the interval that the phase voltage is positive and the line current is negative, the reactive current flows to the source through the bypass diodes. Also the six-stepped wave shape is phase shifted from the line voltage by 30°. The motor phase current lags the voltage due to the presence of motor reactance.

The output voltage does not depend on the load. However, the duration of each switch conduction is dependent on the power factor of the load. Even though the switches are in their on-state for 180°, due to the lagging power factor of the load, their actual conduction interval are smaller than 180°. As the power factor of the load

decreases, the diode conduction interval will increase, and the switch conduction interval will decrease.

The fourier analysis of the output voltage harmonics is done using both experimental data and SPICE3 simulation and is given in Appendix E. The 5^{th} and 7^{th} voltage harmonics are dominant and the simulated and experimental data are quite comparable.

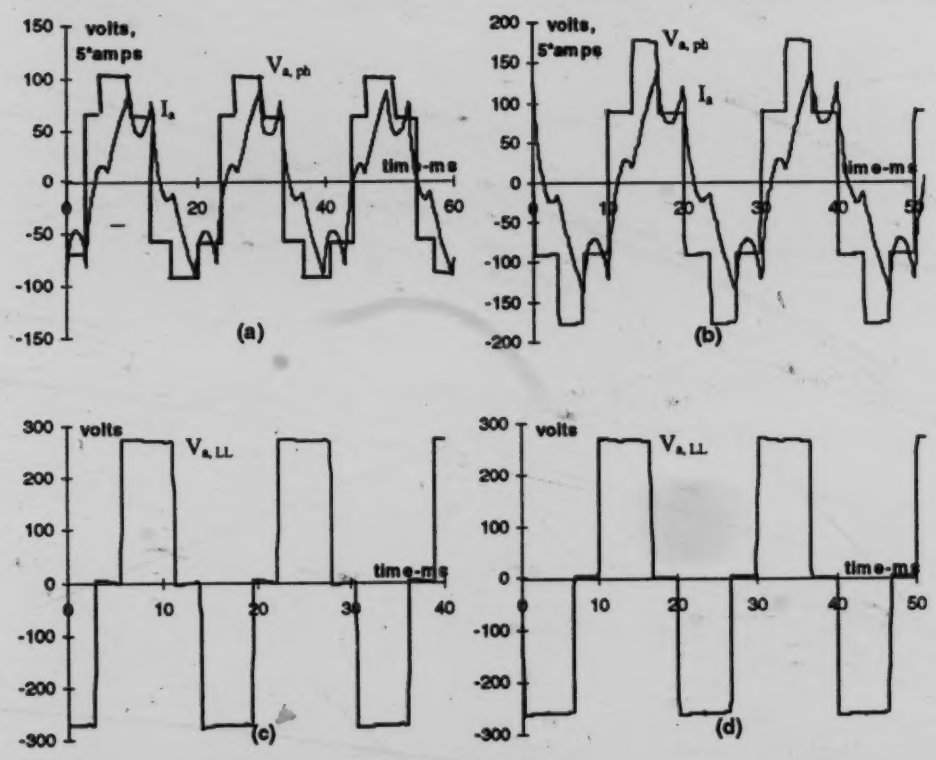


Fig. 4.3 Simulated and experimental waveforms for square wave VSI (a) simulated phase voltage and line current, (b) experimental phase voltage and line current, (c) simulated line-to-line voltage, (d) experimental line-to-line voltage.

4.2 Pulse Width Modulated Voltage Source Inverter

The square wave inverter suffers from the drawback that it does not have any control on the output voltage thus requiring a controlled input voltage. The PWM inverter has the provision of control of the output voltage and hence can be supplied

from a fixed dc voltage. Because of a constant dc bus voltage, a number of PWM inverters with their associated motors can be supplied from a common diode bridge and the commutation problem associated with the 6-step thyristor inverter as explained in the previous section is eliminated. These advantages, however are obtained at the expense of a complex control and a higher switching losses due to a higher frequency operation of the switches.

The PWM inverter combines both voltage and frequency control within the inverter itself. It operates with a fixed voltage dc source. One, two or all three of the thyristors in the inverter which conduct at any instant are additionally switched at a high frequency, thus operating also as a chopper. The circuit discussed in the present work uses the Sinewave Modulated PWM in which the switching ratio is continuously changing, usually sinusoidally, to synthesize a nearly sinusoidal motor current [36].

In the Sinewave Modulated PWM technique the output voltage can be synthesized by generating a duty cycle (i.e, varying the switch dwell time over some switching period) which is proportional to the reference output voltage. The reference is a sine wave and it is compared with a triangle carrier wave to generate a sinusoidally-varying duty cycle, see Fig. 4.4.

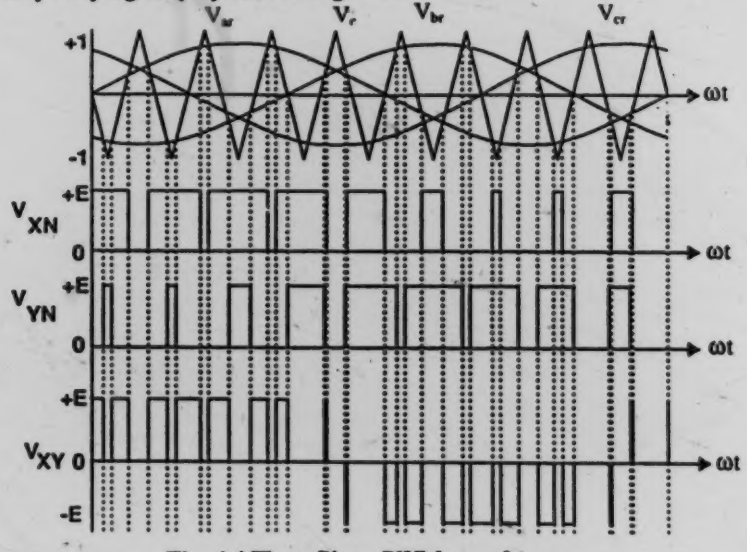


Fig. 4.4 Three-Phase PWM waveforms

The frequency-modulation ratio m_f , which is the ratio of the carrier wave frequency to the sine wave frequency, is kept high because of the relative ease in filtering harmonic voltages at high frequencies [44].

4.2.1 Simulation of PWM voltage source inverter

The circuit model for the square wave inverter has three inverter legs and six switching devices. One of the problems it faces is that when operating at high frequency the simulation runs into convergence problems due to the commutation of the device currents from one inverter leg to the other. Also the clamping diodes result in reverse recovery problem.

The circuit for the PWM voltage source inverter is simplified for simulation purposes. Each leg of the inverter bridge is modeled by a voltage function as shown in Fig.4.5 and is defined as a product of two voltages, one representing the input dc voltage and the other, the PWM switching pattern. The PWM switching pattern is generated by using a B-statement and U-statement that is used to compare a triangular carrier wave with the fundamental frequency sine modulated wave to obtain the natural point of intersection that determine the switching pattern.

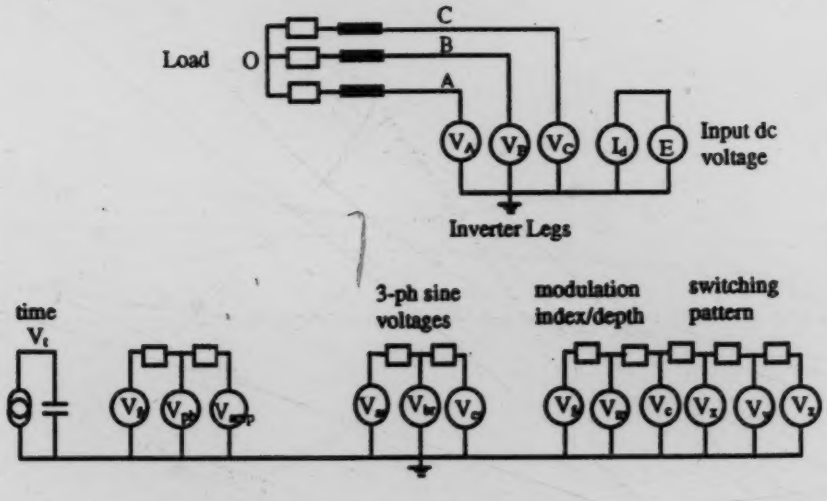


Fig. 4.5 SPICE3 model for PWM VSI

The modeling of the six switching devices with three simple voltage functions simplifies the problem of a complicated circuitry, current commutation from one inverter leg to the other and reverse recovery problems of the diodes.

Switching pattern

The PWM switching pattern is generated by comparing the carrier and reference waves. The reference waves are three phase supply frequency sinusoidal voltages, V_{ar}, V_{br} and V_{cr}. The triangular carrier wave, V_c is generated by the voltage function

$$V_c = \text{asin}(\sin(V_{fc} * V_{time})) \quad (4.5)$$

where V_{fc} is the carrier wave frequency. As seen from Fig. 4.6 the asin function operates on the simple sinusoidal wave and convert it into a triangular sinusoidal wave. V_{fc} is modeled as a constant voltage source.

The comparison of the carrier and reference waves with the help of U-statements generates the following voltage functions, see Fig. 4.7

$$V_x = U(V_{ar}, V_c) \quad (4.6)$$

$$V_y = U(V_{br}, V_c) \quad (4.7)$$

$$V_z = U(V_{cr}, V_c) \quad (4.8)$$

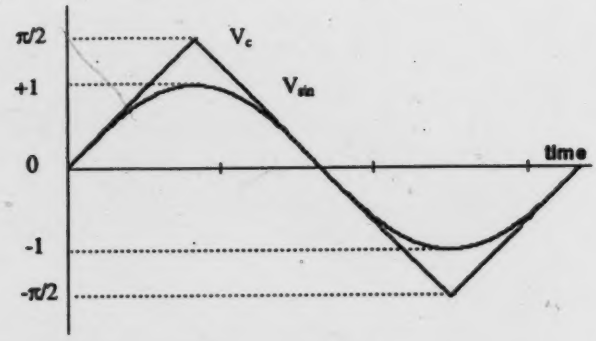
inverter legs

$$V_A = V_{dc} * V_x \quad (4.9)$$

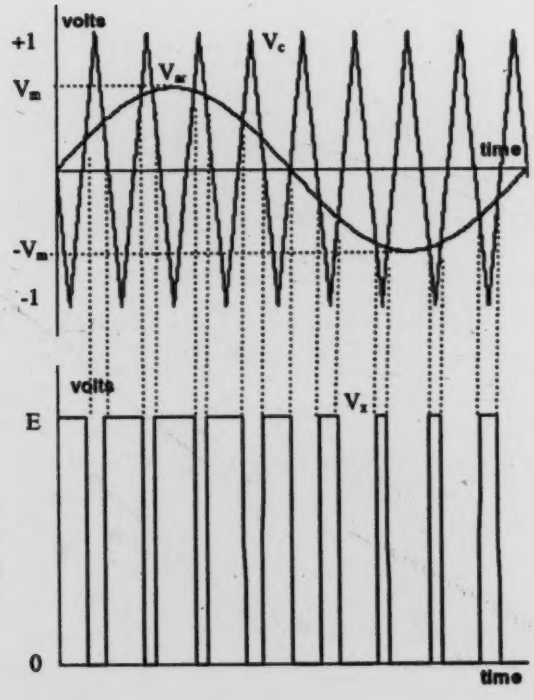
$$V_B = V_{dc} * V_y \quad (4.10)$$

$$V_C = V_{dc} * V_z \quad (4.11)$$

The three inverter legs are modeled with the help of voltage functions which are voltage functions and are a function of the input dc voltage and the switching pattern.



(a)



(b)

Fig. 4.6 PWM Sinewave Generation, (a) Carrier wave generation, (b) PWM waveform

input dc voltage

$$E = 275V \tag{4.12}$$

$$I_d = -I_A * V_x - I_B * V_y - I_C * V_z \tag{4.13}$$

The input is modeled as a constant voltage source of magnitude equal to the rectified voltage. The B-statement is used as a current source feeding the voltage source and is a function of the current flowing in the inverter legs.

Load

The load to the PWM VSI inverter is a R-L load with the same value as that of the induction motor parameters obtained by performing various tests of the Induction Machine, see Appendix D.

The utility interface of the drive consists of a three phase diode bridge rectifier with a capacitor dc-link filter. So the input to the simulation model is a constant dc voltage. Because of the low harmonic content in the output voltage of the diode bridge and in the input current of a PWM inverter, the filter capacitor can be smaller and consequently the drive response is faster than in the case of the square wave inverter.

4.2.2 Waveforms and analysis for PWM VSI Inverter

The load of the inverter is modeled with the same machine parameters as the square wave VSI. Typical simulated and experimental waveshapes are shown in Fig.4.8. As seen from Fig.4.7, undermodulation was used for the simulation purposes.

The maximum available amplitude of the fundamental frequency component is not as high as we desire. This is the natural consequence of the notches as seen from Fig.4.8 (a) (b). The amplitude can be increased by increasing the amplitude modulation ratio m_a, which is the ratio of the peak of the sine wave to the peak of the triangle carrier wave, greater then one. The inverter voltage waveform then degenerates from a pulse-width modulated waveform into a square wave. For our simulation and experimental results we used a m_a less then 1, as seen from Fig.4.7.

It can be seen from Fig.4.8(a),(b) that there are intervals during which all three phases of the load are short circuited and there is no power input from the dc bus, that is the dc current is zero. The output voltage magnitude is controlled by controlling the duration of these short circuit intervals. Such intervals of three-phase short circuit do not exist in a square wave mode of operation. Therefore, the output voltage magnitude

in an inverter operating in a square wave mode must be controlled by controlling the input dc voltage.

It is possible to obtain a line-to-line output voltage that is 15 percent greater than that obtainable when pure sinusoidal modulation is employed by adding a measure of third harmonic to the output of each phase of a three-phase inverter [1]. The line to line voltage is undistorted. The method permits the inverter to deliver an output voltage approximately equal to the ac supply to the inverter. Thus, an induction motor of standard rating with respect to the ac supply can deliver very nearly full power at rated speed when supplied from the inverter.

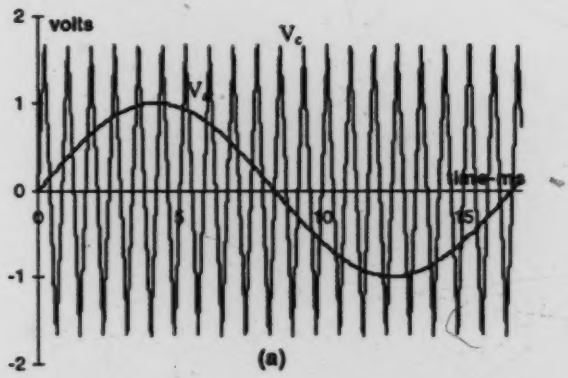


Fig. 4.7 Simulated reference sine wave and triangular carrier wave for PWM VSI

The poor resolution in the experimental waveforms in Fig. 4.8 is due to the limitation of the way data is acquired from LABVIEW. 500 data points are acquired for the oscilloscope screen in this case. Also, the sloping nature of the experimental waveforms is due to the averaging method used in the high resolution function of the oscilloscope.

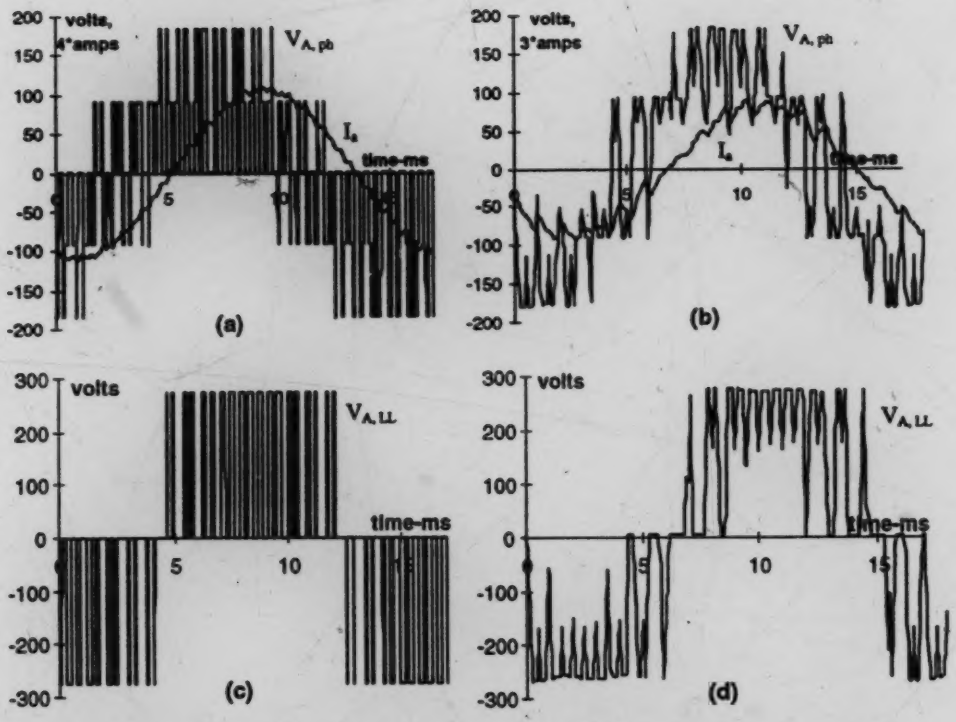


Fig. 4.8 Simulated and experimental waveforms for PWM VSI, (a) simulated phase voltage and line current, (b) experimental phase voltage and line current, (c) simulated line-to-line voltage, (d) experimental line-to-line voltage.

4.3 Three-level PWM inverter

Three-level inverter fed AC drives are increasingly employed in industry and traction applications for higher power, high voltage and high efficiency energy conversion [45]. Typically such drives are rated from several hundred to several thousand horse power. The main advantages of the three-level inverter can be summarized as :

- The voltage of a switching device is clamped to 1/2 V_{dc} thus avoiding serial connections.
- Three-level PWM shifts the first group of voltage harmonics to a frequency band which centers at two times of the modulation frequency. Therefore, it produces

low harmonics in output voltage and current. This allows a low modulation frequency to reduce the switch loss of the inverter and increase efficiency.

- Multilevel voltage waveform in general reduces the dv/dt stress on the motor windings.
- High power rating can be achieved.

Harmonics can be reduced as required through PWM voltage control techniques, but harmonic reduction becomes impossible when the inverter is delivering its full output, at which time the harmonic content of the output waveform is that of a typical square wave, with absence of triplen harmonics.

Typical circuit for a three-level inverter is shown in Fig.4.9. The neutral-point-clamped PWM inverter (NPC-PWM inverter) is suitable for high efficiency motor drive system. Its output voltage contains less harmonics than that of a conventional inverter. (O) indicates the neutral point with respect to the dc source; (S_{11}, S_{14}), (S_{21}, S_{24}), (S_{31}, S_{34}) are main transistors operating as switches for PWM; and (S_{12}, S_{13}), (S_{22}, S_{23}), (S_{32}, S_{33}) are auxiliary transistors to clamp the output terminal potentials to the neutral point potential, together with (D_{11}-D_{32}) .

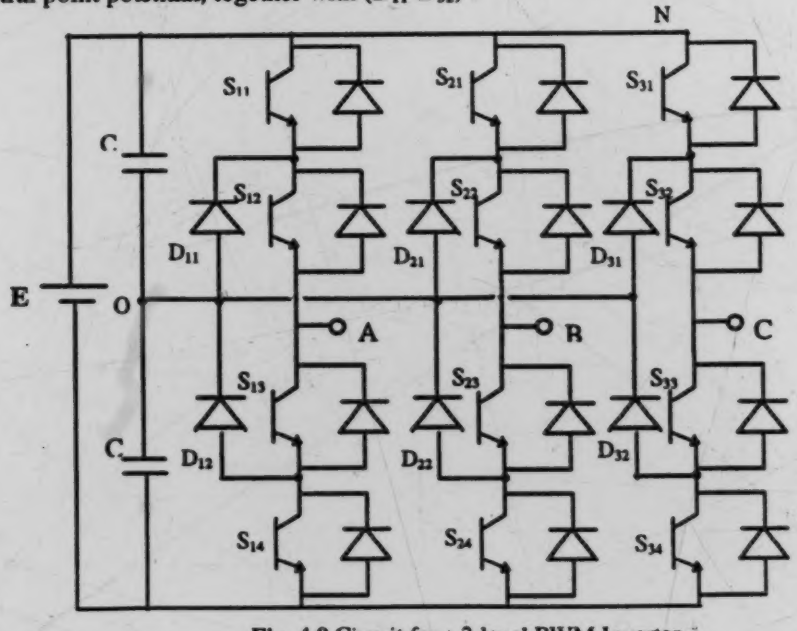


Fig. 4.9 Circuit for a 3-level PWM Inverter

Pulse-width modulation for the three-level VSI is done by comparing a triangular carrier wave with a sinusoidal reference wave as shown in Fig. 4.10.

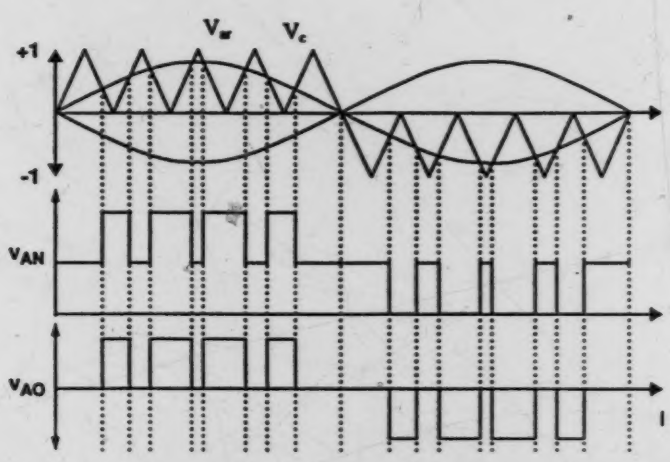


Fig. 4.10 PWM waveform for 3-level VSI

Fig.4.11 shows a typical output voltage waveform of a 3-level inverter. It can be seen that when switching at low frequencies, a specific duration of a zero interval θ, can eliminate any one specific harmonic [25]. The Fourier expression for the waveform can be written as

$$e = \frac{4}{\pi n} \Sigma V \cos n\theta \sin n\omega t \qquad (4.14)$$

where V = 0.5 E

if $\theta = 18°$, the fifth harmonic will be zero,

if $\theta = 12.85°$, the seventh harmonic will be zero, etc.

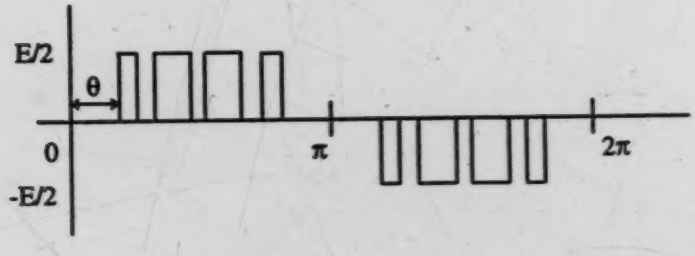


Fig. 4.11 Typical output waveform for 3-level inverter

4.3.1 Simulation of Three-level PWM inverter

The SPICE3 simulation for the 3-level PWM inverter has the same basic model as that of the 2-level inverter. The input to the inverter is taken from a 12-pulse diode bridge rectifier with a split capacitor arrangement as discussed in Chapter 2. The output of the inverter is modeled using the same IM stator parameters as in the 2-level inverter. The SPICE3 schematic for the 3-level inverter is very much similar to the 2-level inverter in Fig.4.4, the only difference being the functions used to generate the switching pattern. The input to the inverter is taken from a 12-pulse split capacitor. The +E, 0 and -E voltages of the dc-link are fed to the voltage functions in the inverter legs, so that the B-statements are voltage functions and are the product of the dc-link voltage and the switching pattern. Detailed model of the 3-level inverter is explained in section 7.3.1.

4.3.2 Waveform and analysis of 3-level PWM inverter

Typical simulated waveforms of the 3-level PWM inverter is shown in Fig. 4.12. The waveforms in Fig. 4.12 show that the voltage waveform have a positive, negative and zero reference. The auxiliary transistors switch complementary to the main transistors. With such control, each output terminal potential is clamped to the neutral potential in the off period of the PWM control as seen from Fig. 4.12 (a). If we compare these waveform with the conventional 2-level PWM inverter, we can easily recognize that the output terminal potential of the conventional PWM inverter vary between +E/2 and -E/2, but those of the NPC-PWM inverter vary between +E/2 and 0 or -E/2 and 0. This reduces the voltage stress on the switching devices and avoids serial connection of the devices.

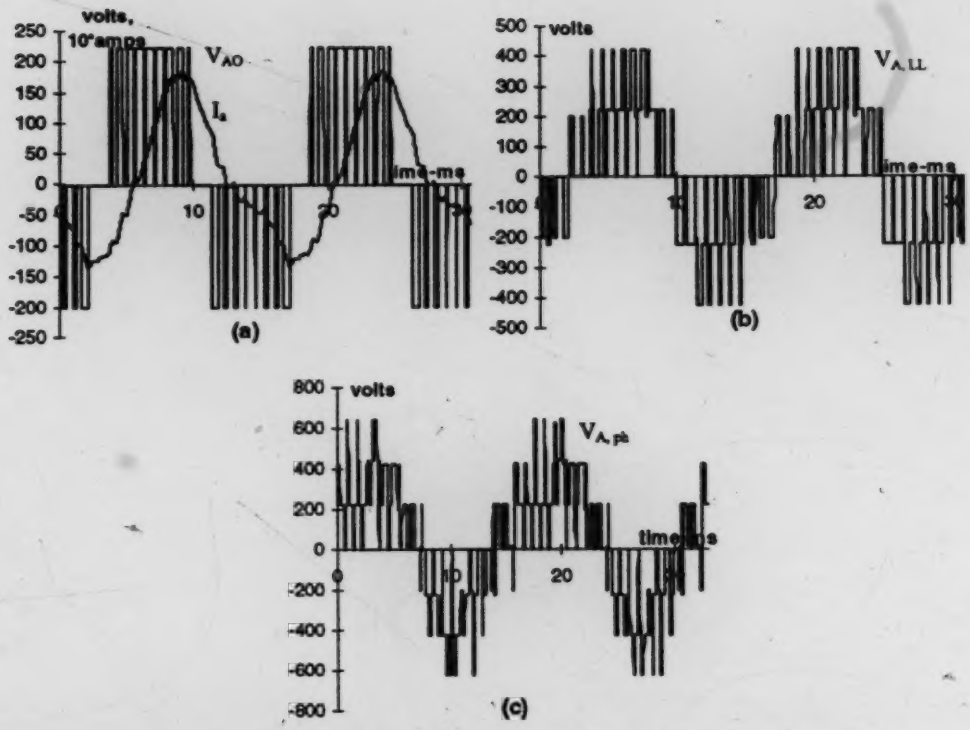


Fig. 4.12 Simulated waveform for 3-level PWM inverter, (a) phase to neutral voltage and line current, (b) line-to-line voltage, (c) phase voltage.

The zero interval duration as shown in Fig.4.11 was adjusted to approximately 18° to eliminate the 5th harmonic at low switching frequencies. The Fourier analysis which is done using SPICE3 is given in Appendix E. It gives the 5th harmonics in the output voltage for the 3-level inverter to be as low as 1.7 %. On the other hand, the 5th harmonics in the output voltage for the 2-level PWM inverter for the same switching frequency is 9.44 %.

Chapter 5

CURRENT SOURCE INVERTER

Inverters convert direct current to variable frequency alternating current. In a Current Source Inverter (CSI), the dc input appears as a dc current source (ideally with the internal impedance approaching infinity). The CSI is presently used for very high power ac motor drives. This chapter discusses a PWM Current Source Inverter (CSI). The simulated waveforms have been presented. A generalized structure of a simple controller for a current source inverter is also explained.

5.1 6-pulse, 2-level PWM Current Source Inverter

A general power circuit for a current-fed inverter, supplied from a phase-controlled rectifier is shown in Fig.5.1. A variable dc link voltage is generated by the phase controlled rectifier. A series inductance in the dc-link causes a stiff dc current to be fed to the inverter. Although an infinite value of the inductor is desirable for an ideal current source, the cost and size constraints limit the inductance to a reasonable limit. At any instant one upper thyristor and one lower thyristor remains in conduction. Capacitors are connected at the output of the inverter to absorb high frequency harmonics associated with the PWM current source inverter output current.

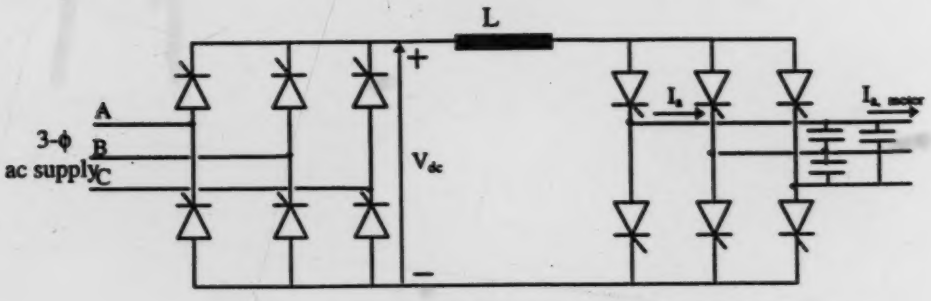


Fig. 5.1 Circuit diagram for Current Source Inverter

As shown in Fig.5.1 above, the PWM CSI in the present work is fed by a current source obtained by the rectification of a three phase ac mains voltage. The current source of the dc link is provided by a reactor which is large enough so as to act as a current source with very little ripple. Current fed into the inverter is converted into three ac line currents by the appropriate gating pattern of the inverter switches. Current harmonics are absorbed by the output filter so as to provide sinusoidal load current and voltage. In a current source inverter, the fundamental component machine current can be varied by controlling the input current of the inverter. Therefore, PWM is only required to improve the current waveforms.

5.1.1 Simulation of 6-pulse, 2-level PWM CSI

The modeling of the PWM Current Source Inverter is done in much the same way as the PWM VSI. The six switching devices are modeled with the help of three current functions, each representing an inverter leg, see Fig. 5.2. The input to the inverter is a constant current source. Each B-function in the inverter leg is a product of the PWM switching pattern and the constant current. The current flowing in the inverter legs is reflected back in the input of the inverter. The output of the inverter has capacitors to absorb the current harmonics. Capacitors are also required to absorb the overvoltages which occur when the current in the switching device is cut off. The load to the inverter is an induction motor and the resistance and reactance values in the present model is chosen to be the same as the motor stator parameters as given in Appendix D. The SPICE3 schematic for the PWM CSI along with its netlist is given in Appendix G.5.

The PWM switching pattern for the CSI is generated as shown in Fig. 5.3. where half carrier cycle is considered. Three phase sinusoidal reference waves are compared with a triangular carrier wave varying at the modulating frequency.

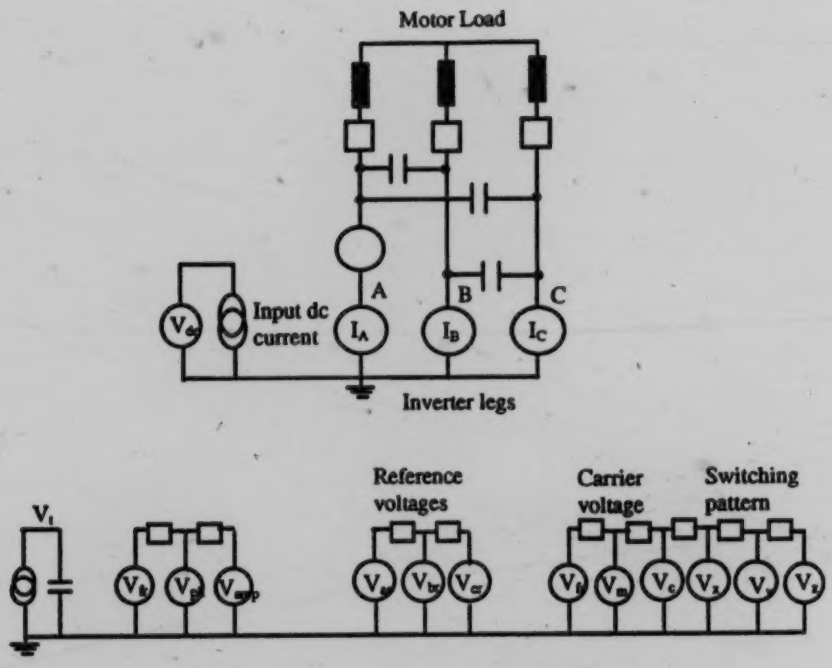


Fig. 5.2 SPICE3 model for PWM CSI

switching pattern

$$V_x = U(V_{ar}, V_c) \quad (5.1)$$

$$V_y = U(V_{br}, V_c) \quad (5.2)$$

$$V_z = U(V_{cr}, V_c) \quad (5.3)$$

The switching pattern is generated by comparing a triangular carrier wave varying at the modulating frequency with the sinusoidal reference wave.

inverter legs

$$I_A = I_{dc} * V_{xy} \quad (5.4)$$

$$I_B = I_{dc} * V_{yz} \quad (5.5)$$

$$I_C = I_{dc} * V_{zx} \quad (5.6)$$

The three inverter legs are modeled with the help of B-statements which are current functions that are a product of the input dc current and the switching pattern, see Fig. 5.3. A current sensor, which is modeled as a dc voltage source of zero magnitude, is in series with the B-statement in one of the inverter legs. This current

function helps to measure the inverter current and compare it with the output motor current.

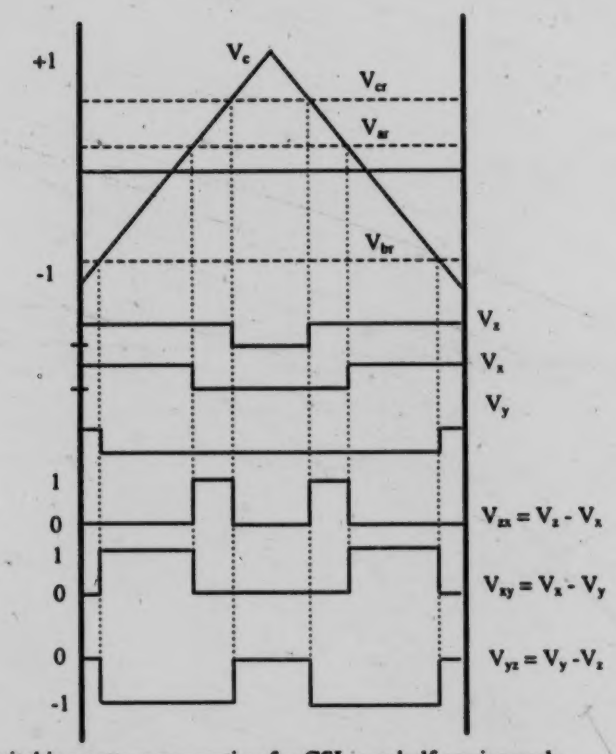


Fig. 5.3 Switching pattern generation for CSI over half carrier cycle.

input

$$I_{dc} = 100A \quad (5.7)$$

$$V_d = V_A * V_x + V_B * V_y + V_C * V_z \quad (5.8)$$

The input is modeled as a constant current source of magnitude equal to 100A for purpose of simulation. The B-statement is used as a voltage function and is a function of the voltages across the inverter legs.

One of the major advantages of using voltage or current functions to represent the switching devices is that it eliminates the use of other available library devices like BJT, MOSFET, etc. These devices are described as non-linear controlled source by means of functions that contain exponential terms, resulting in slow execution times,

integration process), and occasional convergence problems. The current functions also eliminate reverse recovery problem of the diodes associated with the six switching devices in the inverter.

5.1.2 Waveform and analysis for PWM CSI

As seen from the simulated waveforms of the PWM CSI in Fig.5.4 the inverter output current is the pulsewidth modulated dc link inductor current. The voltage reflected at the input of the inverter is chopped, and is similar to the dc link current in a VSI. The dc bus voltage as seen in Fig. 5.4(c) at the input of the inverter is the output voltage reflected on the dc bus through the operation of the inverter switch.

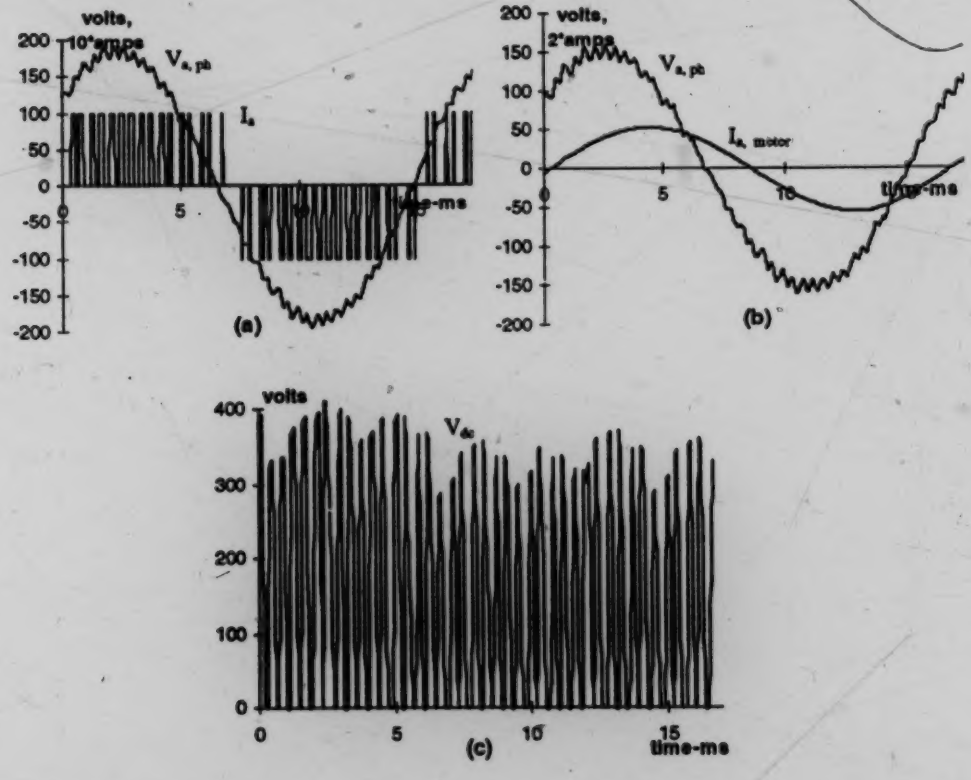


Fig. 5.4 Simulated waveform for CSI PWM, (a) Motor line voltage and CSI line current, (b) Motor phase voltage and motor line current, (c) dc link voltage.

The dc-link voltage is chopped due to the inverter's switching nature. Comparing the CSI line current with the motor line current we can see that the capacitors at the output offer a low impedance path to the higher order harmonics thus making the motor line current sinusoidal. Thus, with the inverter acting as a current source nearly sinusoidal output voltage and current can be obtained.

5.1.3 Harmonic analysis for PWM CSI

Low harmonic contents in both the output voltage and current of a CSI is desired for a number of reasons. Current harmonics cause additional heating of windings, particularly in large motors where skin effect is more significant. Voltage harmonics can increase core losses and rapid rates of changes of voltage with time can increase insulation stress. In addition, these harmonics may cause torque harmonics and acoustic noise.

Harmonic analysis is done for the current harmonics in the CSI line current and the motor line current using SPICE simulation and is given Appendix E. The 5^{th} and the 7^{th} current harmonics get significantly suppressed due the output capacitance. Also the output line current THD improves from 8.79% in the CSI line current to 2.27% in the motor line current.

5.2 Controlled Current Source for a CSI

Strictly speaking, the scheme described above in section 5.1 does not act as a current source. Any change in the machine impedance, with a change in slip, changes the magnitude of I_d and machine phase currents. If both the waveform and the magnitudes of machine currents are to be made independent of changes in machine operation, then the magnitude of I_d should also be maintained constant. This is achieved by closed-loop control scheme of I_d. Fig. 5.5 shows the current source inverter scheme incorporating the closed loop current control. The actual current, I_d is compared to the reference value, I_d^*. The error is processed in a controller to adjust the rectifier firing angle to eventually make the actual current equal to the reference.

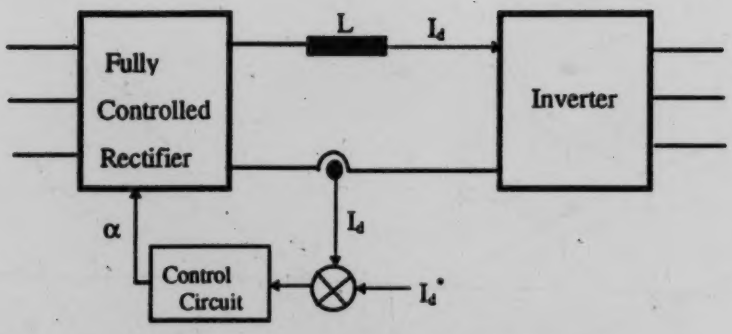


Fig. 5.5 Block diagram for control scheme of the current source

Since the dc current is continuously adjusted, the dc voltage is practically constant and independent of the load fluctuations. This feature leads to a constant input current displacement factor and thereby a constant global power factor.

Chapter 6

INDUCTION MOTOR

The motors commonly used in variable speed drives are induction motors, dc motors and synchronous motors. For the purpose of our work the induction motor has been used. The d-q axis theory is used to model the induction machine and the use of B-statements to incorporate the complex equations is shown. The induction motor is modeled for SPICE3 simulation and its transient response is compared with experimental results. A motor model for constant voltage per hertz (V/f) operation for the induction motor is obtained and the command interpreter is used for obtaining various curves at different values of V/f.

6.1 Induction Motor drive

Induction motors, particularly the squirrel-cage type induction motor, are widely used in variable speed drives for a number of advantages. Some of them are ruggedness; lower maintenance requirements; better reliability; lower cost, weight, volume and inertia.

When operated directly from the line voltages (60Hz utility input at essentially constant voltage), an induction motor operates at a nearly constant speed. However, by means of power electronic converters, it is possible to vary the speed of an induction motor. In practice, the inverters used in variable speed drives produce three-phase line voltages or currents, that are not perfectly sinusoidal and contain higher frequency components that are harmonics of the fundamental frequency.

6.1.1 Induction motor modeling

The induction motor is modeled using the two-axis or d-q theory [40]. In this theory the time-varying parameters are eliminated and the variables and parameters are expressed in orthogonal or mutually decoupled direct(d) and quadrature(q) axis. The

d-q dynamic model of a machine can be expressed in either a stationery or a rotating reference frame. In a stationery reference frame, the reference d and q axis are fixed on the stator, whereas in a rotating reference frame these are rotating. The rotating reference frame may be either fixed to the rotor or move at synchronous speed.

The two-axis machine equation can be formulated in various reference frames. However for the cylindrical rotor squirrel-cage induction motor, the stator fixed axes prove more convenient, since the motor model can then be defined in terms of the physically existing stator voltages and currents. This allows the interface between the motor model and the rest of the power electronic system to be easily created, without the need for the user to analytically determine the interaction that arises between the power electronics and the motor.

Considering only the stator supply voltages we derive a transformation relationship between the A-B-C axes and the d-q axes, where both are in the stationery reference frame as shown in Fig.6.1. The other quantities, such as current and flux can also be transformed in a similar manner.

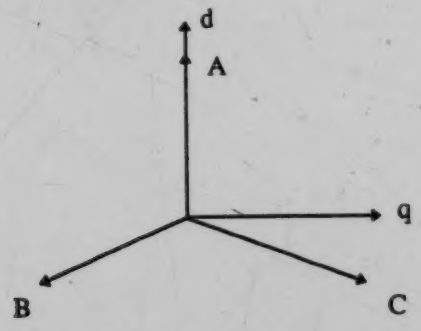


Fig. 6.1 Stationery A-B-C to d-q axes transformation

The phase voltages in terms of d and q voltages can be written in the matrix form as

$$\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta & 1 \\ \sin(\theta-120) & \cos(\theta-120) & 1 \\ \sin(\theta+120) & \cos(\theta+120) & 1 \end{bmatrix} \bullet \begin{bmatrix} Vq \\ Vd \\ Vo \end{bmatrix} \qquad (6.1)$$

where the angle θ is arbitrary between the two sets of axes and V_o is the zero sequence component. For balanced three-phase condition, the zero-sequence components does not exist.

Choosing the angle $\theta = 0$, axis A is coincident with axis d. Simplifying, we get the following relations

$$V_a = V_d \tag{6.2}$$

$$V_b = -\frac{1}{2} V_d - \frac{\sqrt{3}}{2} V_q \tag{6.3}$$

$$V_c = -\frac{1}{2} V_d + \frac{\sqrt{3}}{2} V_q \tag{6.4}$$

$$V_d = (2V_a - V_b - V_c) / 3 \tag{6.5}$$

$$V_q = (V_c - V_b) / \sqrt{3} \tag{6.6}$$

If we consider separate d and q per phase equivalent circuit for the induction motor, the flux linkage expression in terms of the currents can be written as

$$\psi_{qs} = L_{ls} i_{qs} + L_m (i_{qs} + i_{qr}) \tag{6.7}$$

$$\psi_{qr} = L_{lr} i_{qr} + L_m (i_{qs} + i_{qr}) \tag{6.8}$$

$$\psi_{ds} = L_{ls} i_{ds} + L_m (i_{ds} + i_{dr}) \tag{6.9}$$

$$\psi_{dr} = L_{ls} i_{dr} + L_m (i_{ds} + i_{dr}) \tag{6.10}$$

The development of torque by the interaction of air gap flux and rotor mmf is given by the expression

$$T_e = \frac{3}{2} (P/2) \psi \times I_r \tag{6.11}$$

or in terms of d-q components as

$$T_e = \frac{3}{2} (P/2) (\psi_{dm} i_{qr} - \psi_{qm} i_{dr}) \tag{6.12}$$

$$= \frac{3}{2} (P/2) (\psi_{dm} i_{qs} - \psi_{qm} i_{ds}) \tag{6.13}$$

$$= \frac{3}{2} (P/2) (\psi_{ds} i_{qs} - \psi_{qs} i_{ds}) \tag{6.14}$$

$$= \frac{3}{2} (P/2) L_m (i_{qs} i_{dr} - i_{ds} i_{qr}) \tag{6.15}$$

Also, the motor speed is related to the torque as

$$T_e - T_L = \frac{2}{P} J \frac{d\omega_r}{dt} \qquad (6.16)$$

where T_L is the load torque and J is the induction motor inertia

Equation (6.15) and (6.16) give the complete model of the electromechanical dynamics of the induction motor in terms of the d-q components. The non-linearity of the model is very evident. The obtained model using the transformation equations can be simulated for studying the transient and steady state performances.

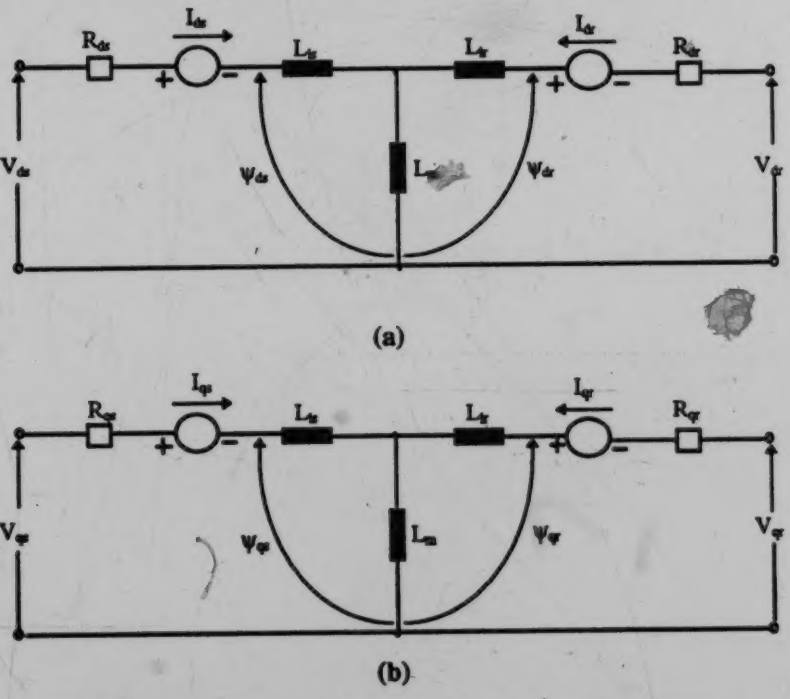


Fig. 6.2 d-q equivalent circuits, (a) d-axis circuit, (b) q-axis circuit

V_{ds} and V_{qs} are defined by equations(6.5) and (6.6) respectively. Similarly, V_{dr} and V_{qr} are defined by equations(6.8) and (6.10) respectively.

6.1.2 SPICE3 simulation of Induction motor

The various equation in section 6.1.1 are used in simulating the induction motor in SPICE3. The availability of the B-statement and the U-statement facilitate the modeling of the complex equations. The parameters used in the d-q equivalent circuit are the same as in the motor per phase equivalent circuit, see Fig.6.3 such that :

$$R_s = R_{ds} = R_{qs} \tag{6.17}$$

$$L_s = L_{ds} = L_{qs} \tag{6.18}$$

$$R_r = R_{dr} = R_{qr} \tag{6.19}$$

$$L_r = L_{dr} = L_{qr} \tag{6.20}$$

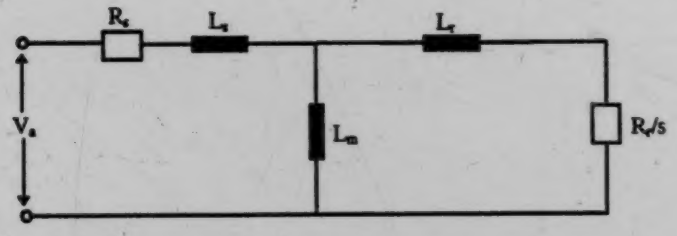


Fig. 6.3 Per-phase equivalent circuit for Induction Motor

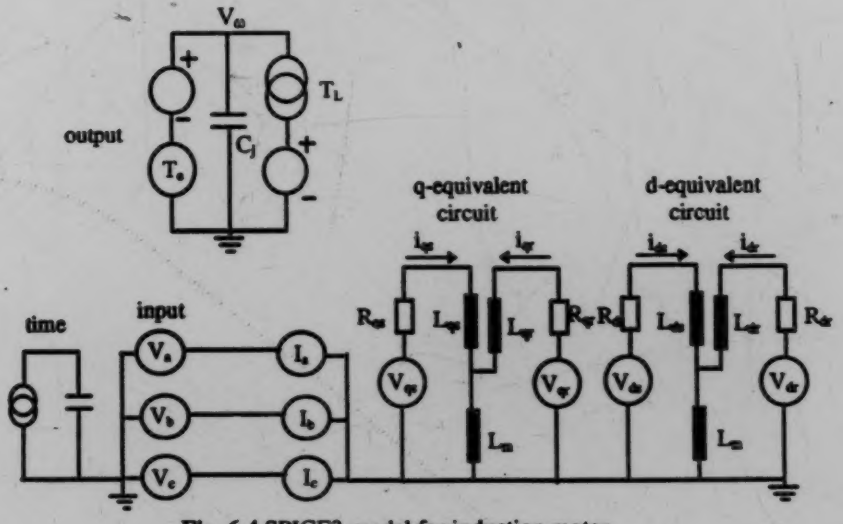


Fig. 6.4 SPICE3 model for induction motor

For the induction motor, two separate d and q per phase equivalent circuits are considered. The input to the motor is the three phase voltages V_a, V_b and V_c. As seen from the SPICE3 model in Fig.6.4, the input to each of the per phase equivalent circuit are the respective d and q voltages as defined by Equation (6.5),(6.6). The currents flowing in the stator of the d and q equivalent circuits are defined by the corresponding current expression similar to Equation(6.2),(6.3),(6.4) and are reflected back to the input side of the motor. Similarly the current flowing in the rotor of the d and q equivalent circuit are reflected back to the output side of the motor. The stator and rotor parameters used in the simulation are same as those of the actual motor used in the experimental setup. These values are found by various experimental tests as given in Appendix D.

The output of the motor is defined by the Equation(6.16). It is modeled as a B-statement in parallel with a capacitor. The B-statement is a current function defined by Equation (6.15) and represents the electromagnetic torque, T_e. The load torque, T_L is simulated by a constant current source drawing current out of the capacitor. The capacitor, C_j is the measure of the system inertia, J. The voltage, V_ω across the capacitor would thus give the speed, see Equation (6.16).

The SPICE3 schematic for the induction machine along with its netlist is given in Appendix G.6.

6.1.3 Waveforms and analysis for Induction Motor

Fig.6.5 present the simulation results for direct-on-line (DOL) starting of the motor. The corresponding experimental results in Fig.6.5(d) show good agreement with the simulation results, thus confirming the validity and accuracy of the motor model. As illustrated, large transient overshoots of torque and current result and persist for a number of cycles before final steady-state conditions are established.

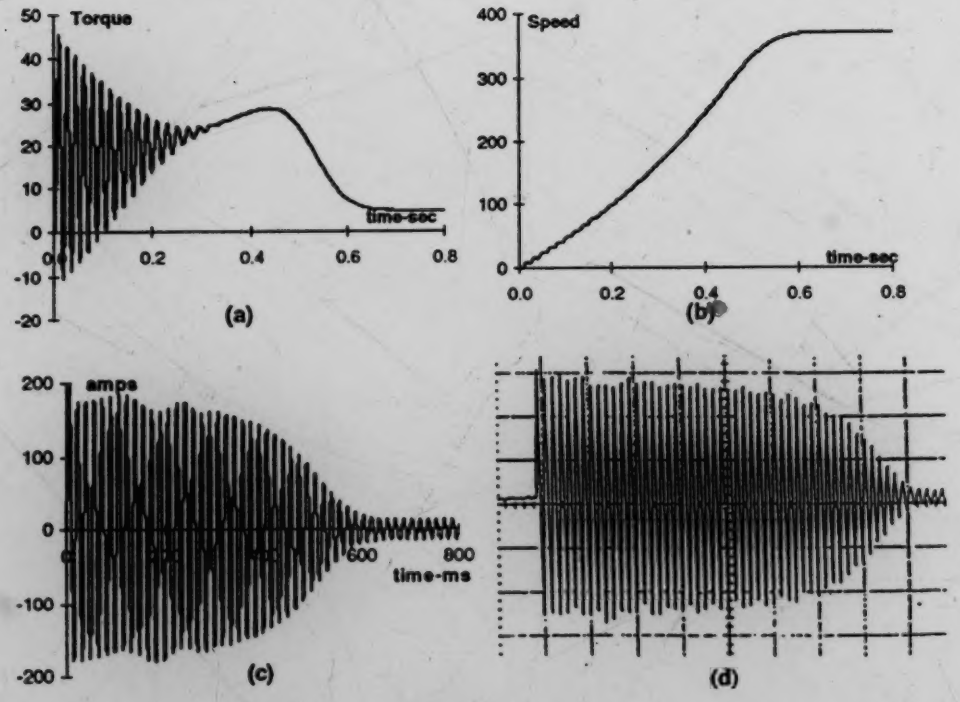


Fig. 6.5 Simulation waveforms for Induction Motor, (a) Starting torque, (b) Speed curve, (c) Starting current, (d) experimental Starting current (200A/div).

6.2 Constant voltage/frequency operation

In an induction machine, the voltage induced in the stator is directly proportional to the product of the supply frequency, f and the air-gap flux, ϕ_{ag}. If the stator drop is neglected, the motor terminal voltage can be considered proportional to the product of the frequency and the flux. Any reduction in the supply frequency, without a change in the terminal voltage, causes an increase in the air-gap flux. Induction motors are designed to operate at the knee point of the magnetizing characteristics to make full use of the magnetic material. Therefore, the increase in flux will saturate the motor. Similarly, a decrease in flux is also avoided to retain the torque capability of the motor. Therefore, the variable frequency control below the rated frequency is generally carried out by reducing the machine phase voltage, V along with

the frequency, f in such a manner that the flux is maintained constant assuming the stator impedance is negligible.

$$\phi_{ag} = k.\ E_{ag}/f = K.V/f \qquad (6.21)$$

The motor speed can be varied by controlling the applied frequency f, and the air-gap flux should be kept constant at its rated value by controlling the magnitude of the applied voltages in proportion to f. If an induction motor is controlled in such a manner, then the motor is capable of supplying its rated torque while the slip frequency (f_{sl}), rotor current, motor supply current and the percentage losses in the rotor circuit all remain within their respective rated values.

6.2.1 SPICE3 simulation of constant V/ f operation

The simulation for the constant V/f operation is done using the model of the induction motor as explained in section 6.1.1 and modifying it for steady state operation. To minimize the starting transient in the motor current , the current in the magnetizing inductor in both the d and q equivalent circuits are initialized. For the d equivalent circuit, the current flowing in supply phase a is simply the primary current, I_d. The current in the magnetizing inductor for the d equivalent circuit is initialized to a value given by the equation below

$$I_{initial} = \frac{-0.816V_{LL}}{2\pi f\,(L_s + L_m)} \qquad (6.22)$$

The corresponding current in the q equivalent circuit is 90° phase shifted from the d equivalent circuit. Thus the current in the q equivalent circuit goes through zero at the instant the corresponding current in the d equivalent circuit goes through its peak maximum. The magnetizing current in therefore initialized to zero for the q equivalent circuit. These currents are initialized using the IC (initial current) statement.

The output torque-speed model is modified from the existing model of section 6.1.1 by removing the capacitor and the constant current source feeding the capacitor. The speed of the motor is fixed to 1800 rpm (188 rad/sec). This is modeled by a constant voltage source of magnitude 188. The output model is thus a B-statement

which is a current function of the rotor currents feeding a constant voltage source. The current function represents the motor torque and the voltage across the voltage source represents the motor speed.

The .CONTROL statement of the command interpreter is used to generate the various curves using the above modified model. The while loop is used to vary slip from 0 to 1 in steps of 0.01. Data is generated for different values of V/f from 0.2 to 1 in steps of 0.2. The run file along with the SPICE3 netlist file is given in Appendix G.9 and is quite self-explanatory.

6.2.2 Analysis of constant V/f operation curves

The various curves obtained using the run file are shown in Fig. 6.6. Fig. 6.6(a) and (c) show the variation of torque and rotor current with speed. At high values of motor speed i.e low slip, torque and rotor currents vary linearly with speed. As speed becomes less, torque and rotor current no longer increases linearly with speed for the following reasons: (1) rotor circuit inductive reactance term is no longer negligible as compared to the rotor resistance, (2) large values of rotor current and hence large stator current cause significant voltage drop across the stator winding impedance causing ϕ_{ag} (= E_{ag}/f) to decline for a fixed supply input voltage at a frequency f [39].

For small values of slip i.e large speeds, keeping ϕ_{ag} constant results in a linear relationship between torque and slip frequency, f_{sl} at any value of f:

$$T = k f_{sl} \tag{6.23}$$

Since f is varied, it is preferable to express torque as a function of the slip speed ω_{sl}.

$$\omega_{sl} = \frac{f_{sl}}{f}\omega_s = \frac{4\pi f_{sl}}{p} \tag{6.24}$$

therefore,

$$T = k' \omega_{sl} \tag{6.25}$$

The torque-speed characteristics shift horizontally in parallel as seen in Fig. 6.6(a) for five different values of f. Considering the two frequencies 60Hz and 48Hz,

the synchronous speeds ω_{s1} and ω_{s2} are in proportion to 60Hz and 48Hz. If an equal load-torque is to be delivered at both these frequencies, from Eq.6.23, $\omega_{sl1} = \omega_{sl2}$. Therefore, in the torque speed plane, equal torques and equal slip speeds result in parallel but horizontally shifted characteristics. It can be seen from Fig. 6.6(c) that the motor starting current can be limited by choosing a lower frequency setting. With a constant magnetizing current due to constant ϕ_{ag}, the stator current is kept from becoming large.

Fig. 6.6(b) and (e) show the variation of torque and input power respectively with increasing motor current and have similar characteristics. Torque varies as the square of the rotor current. The pull-out torque decreases with decreasing frequency setting. A small magnetizing current exists for low speeds at zero torque. Fig. 6.6(d) shows that the variation of power factor with increasing current is almost identical for all V/f settings. Power factor peaks to about 0.96 at approximately 30A for all frequency settings. The efficiency of the motor peaks for all frequency setting at a motor current of 18A as seen from Fig. 6.6(f) and decreases rapidly for increasing current. Large motor current amount to larger copper loss, thus decreasing efficiency.

As seen from Fig. 6.6(a), low frequency of operations, near zero speed causes low torque capability. The stator voltage tends to be zero and it will essentially be absorbed by the stator resistance. The effect of the stator resistance can no longer be neglected. Therefore, an auxiliary voltage boost is required to overcome the effect of stator resistance so that the rated air-gap flux and full torque becomes available up to zero speed.

The various curves in Fig. 6.6 are verified by an equation-based simulation using the per-phase equivalent circuit in Fig. 6.3, thus validating the d-q axis model for the induction machine. The Mathematica simulation run file is included in Appendix G.9 along with the SPICE3 run file.

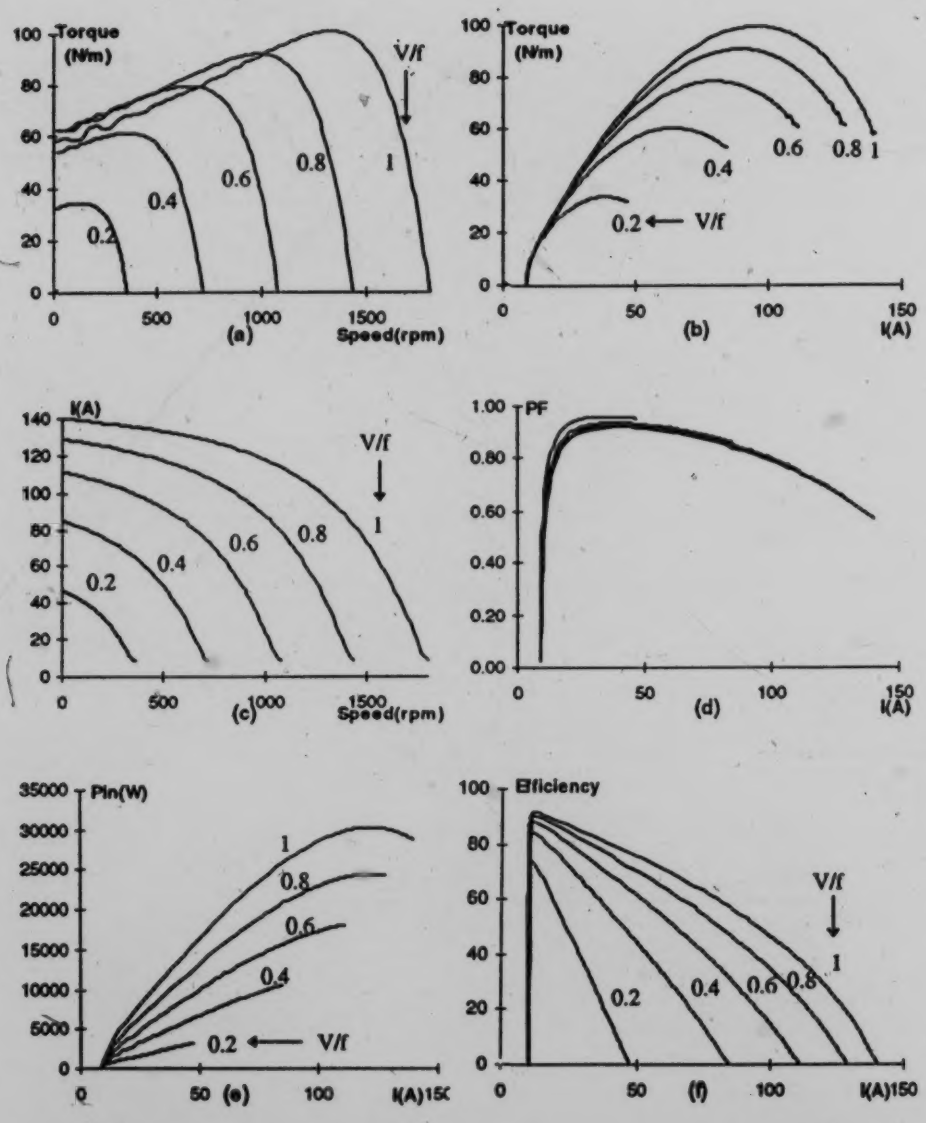


Fig. 6.6 Constant volts per hertz curves for Induction Machine, (a) Torque Vs Speed, (b) Torque Vs Current, (c) Current Vs Speed, (d) PF Vs Current, (e) Input power Vs Current, (f) Efficiency Vs Current.

Speed control by means of frequency (and voltage) variation also allows the capability to operate the motor not only at speeds below the rated speed, but also at above the rated speed. This capability is very attractive in many applications, since

most induction motors, because of their rugged construction can be operated up to twice the rated speed without mechanical problems [39].

Chapter 7

VARIABLE SPEED DRIVE

For the control of induction motors, a fixed frequency ac supply with variable voltage or a variable frequency ac supply with variable voltage or current is required. Variable speed drives utilizing an ac motor fed with variable frequency, three-phase ac derived from an inverter, are encountered with increasing frequency. This chapter discusses the general features of a variable speed drive with emphasis to the PWM inverter drives. The SPICE3 simulation of a 12-pulse, 3-level PWM VSI drive is presented. The usefulness of SPICE3 for simulation of large drive topologies has been explained.

7.1 Selecting drive components

A match between the motor and the power electronic converter is very important for motor drives [39]. The power electronic converter topology and its control depends on the type of motor drive selected. In general the power electronic converter provides a controlled voltage to the motor in order to control the motor current and hence the electromagnetic torque produced by the motor.

A motor can supply substantially large peak torque provided that the peak torque is small compared with the thermal time constant of the motor. A peak torque requires a corresponding peak current from the power electronic converters. The current capability of the power semiconductor devices used in the converter is limited by the maximum junction temperature within the device. The current rating of the power electronic converter must be selected based on both the rms and peak values of the torque that the motor is required to supply.

Motors produce a counter-emf e, that opposes the voltage v applied to it, as shown in the simplified drive circuit in Fig.7.1. The rate at which the motor current and hence

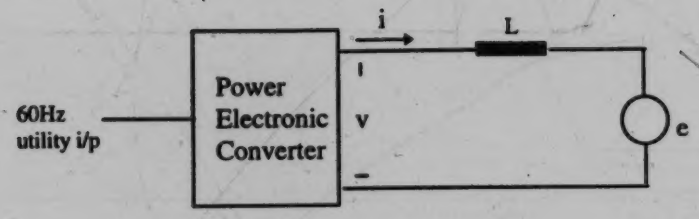


Fig.7.1 Simplified circuit of a motor drive

the torque can be controlled is given by

$$\frac{di}{dt} = \frac{v - e}{L} \qquad (7.1)$$

where L is the approximate inductance presented by the motor to the converter.

To be able to quickly control the motor current and hence its torque, the output voltage v of the power electronic converter must be reasonably greater than the counter-emf e. The magnitude of e in a motor increases linearly with the motor speed, with a constant flux in the air gap of the motor. Therefore, the voltage rating of the power electronic converter depends on the maximum motor speed with a constant air-gap flux.

For the motor current to respond quickly, the motor inductance L should be small in equation 7.1. Also, the steady state ripple in the motor current should be as small as possible to minimize the motor loss and the ripple in the motor torque. A small current ripple requires the motor inductance to be large. Because of the conflicting requirements on the value of L, the ripple in the motor can be reduced by increasing the converter switching frequency. However, the switching losses in the power electronic converter increase linearly with the switching frequency. Therefore, a reasonable compromise must be made in the motor inductance and the switching frequency.

7.2 VSI and CSI Drive Topologies

The basic concept for both the VSI and CSI drive topologies is the same. The utility input is converted into dc by means of either a controlled or an uncontrolled rectifier and then inverted to provide three phase voltages and currents to the motor, adjustable in magnitude and frequency. Inverters used for this purpose should, in addition to regulate the frequency in accord with the desired speed, also regulate the voltage, more or less proportionally with the frequency, so as to maintain the flux density within the machine at the normal operating value [36].

Typical block diagrams of the VSI and CSI drive are given in Fig.1.1 and Fig.1.2 respectively. The input to the drive in the Δ-Δ, Δ-Y transformer, so that their secondaries are phase shifted by 30 degrees. For the PWM VSI, the series connected diode bridge rectifier forms a 12-pulse rectifier that is most suitable for high power application, see Fig.1.1. The rectifier stage is a phase controlled bridge in case of a square wave inverter, where it becomes necessary to control the input to the inverter. In both the VSI, a large dc-bus capacitor is used to make the input to the inverter appear as a voltage source with a very small impedance at the inverter switching frequency. Fig.1.2 shows the block diagram of a CSI drive where a line-voltage-commutated controlled converter is used as the front end. Because of a large inductor in the dc link, the input to the inverter appears as a dc current source.

7.3 12-pulse, 3-level PWM VSI Drive

The 12-pulse, 3-level PWM VSI Drive have increasingly been employed in industry and traction application where high power and efficiency energy conversion is required [29]. This drive is highly suitable for high power and high voltage applications. The 12-pulse rectifier provides a ripple less output voltage. The blocking voltage of each switching device in the 3-level inverter is clamped to half the blocking voltage which allows the use of lower voltage power devices without serial connections.

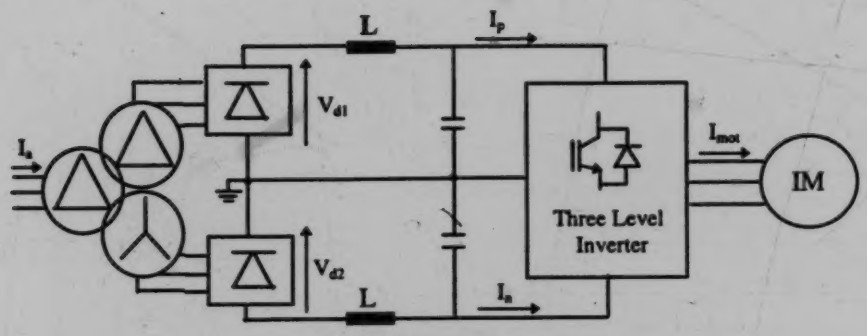


Fig.7.2 Block diagram for 12-pulse, 3-level PWM VSI Inverter Drive

7.3.1 Simulation of 12-pulse, 3-level PWM VSI Drive

One of the advantages of SPICE3 is that a complete power electronic drive system can be simulated in its entirety. SPICE3 is not restricted to the number of nodes in the circuit as was the case with the earlier versions of SPICE and thus large and complex circuits can be easily simulated.

The SPICE3 schematic for the entire drive system along with its netlist is given in Appendix G.7. As seen from the SPICE3 model in Fig.7.4, the input to the drive is the Δ-Δ, Δ-Y transformer which is modeled using separate d and q equivalent circuits. The currents flowing in the transformer primaries are reflected back to the input side. The Δ-Δ, Δ-Y transformer is slightly modified from the one in section 3.2.1. The transformer in this simulation has a common primary and two separate secondaries which is a common transformer connection in the industry, see Fig.7.2. The output of the Δ-Δ, Δ-Y transformer forms the input to the 12-pulse rectifier which has two serially connected 6-pulse diode bridge rectifier. B-statement is effectively used to decouple the output of the transformer and the input of the rectifier.

The output of the rectifier has a split dc capacitor rail. This rectified dc voltage is fed to the 3-level PWM VSI inverter. The current flowing in the legs of the inverter are reflected back to the dc rail with the help of B-statements which are current

functions. The current function in terms of I_p, the positive dc-link current and I_n, the negative dc-link current can be defined with the help of Fig. 7.3.

	SW	A	B	C
I_p	+1	I_A	I_B	I_C
	0	0	0	0
	-1	0	0	0
I_n	+1	0	0	0
	0	0	0	0
	-1	$-I_A$	$-I_B$	$-I_C$

Fig. 7.3 Switching logic for dc-link current

The current function is thus given as

$$I_p = I_{d1} = I_A + I_B + I_C \tag{7.2}$$

$$I_n = I_{d2} = -I_A - I_B - I_C \tag{7.3}$$

The voltage function V_{tri} is used to generate a triangular wave at the modulating frequency, V_{mfr} which is modeled as a constant voltage source.

$$V_{tri} = \text{asin}(\sin(V_{mfr} * V_{time})) + 1.57 \tag{7.4}$$

This is used to generate the three carrier waves, V_{cA}, V_{cB}, V_{cC} with the help of B-statements which are voltage functions. V_{cA} is defined as

$$V_{cA} = u(\sin(V_{fr} * V_{time})) * V_{tri} + (1 - u(\sin(V_{fr} * V_{time}))) * V_{tri} \tag{7.5}$$

U-statements are used to compare the carrier wave with the 3-phase sinusoidal reference waves V_{rA}, V_{rB}, V_{rC} to generate the switching pattern for a 3-level inverter. The resultant voltage function is defined as

$$V_X = u(V_{rA}, V_{cA}) \tag{7.6}$$

The inverter leg is modeled as three B-statements similar to the 2-level case. The B-statements are voltage functions and are the product of the switching pattern

and the capacitor dc-link voltage. The rectified voltage fed to the inverter alternates between +E, 0 and -E. The inverter voltage function for phase A is given as

$$V_A = V_X * V_{d1} + (1 - V_X) * V_{d2} \qquad (7.7)$$

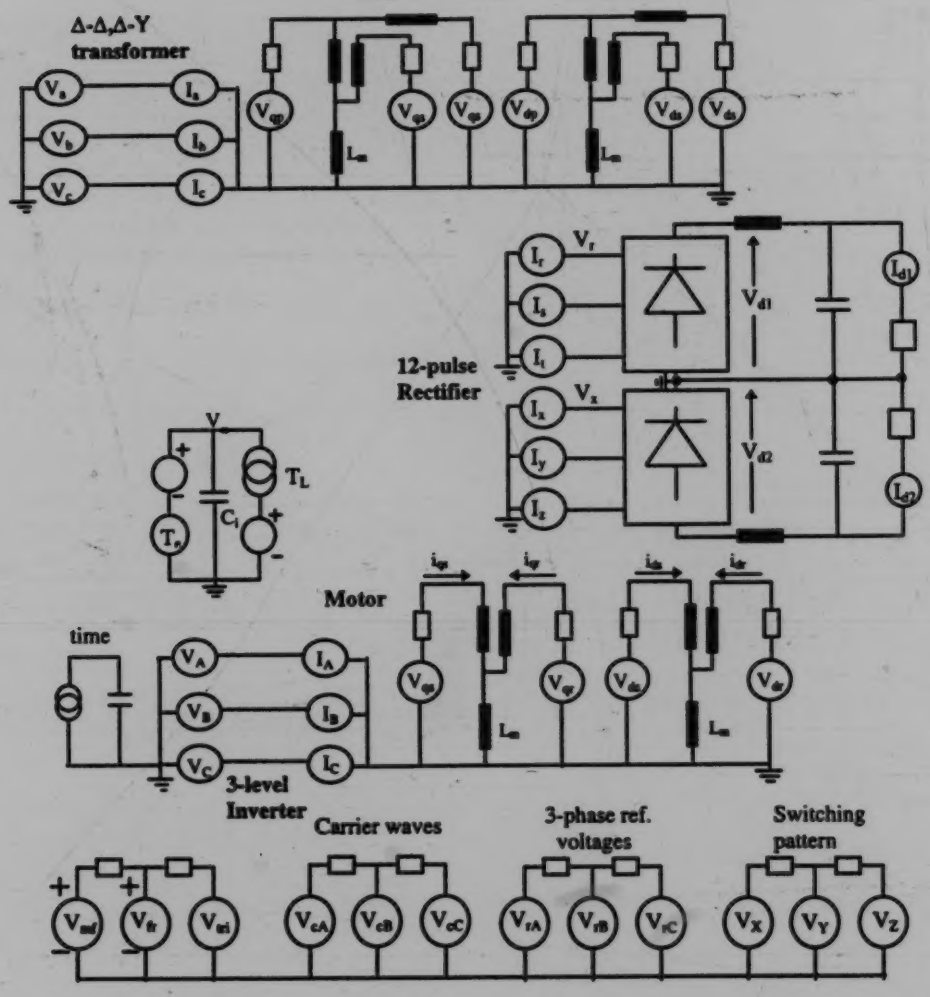


Fig. 7.4 SPICE3 model for the 12-pulse, 3-level PWM VSI drive

The 3-phase output voltage of the inverter is fed to the induction motor. The induction motor is also modeled using the d-q axis theory as discussed in section 6.1.1. The impedance of the rectifier-inverter system as seen by the motor depends on

the conducting states of the power devices and changes according to the PWM switching pattern and current flow. This is automatically accounted for by reflecting the changes in the time-varying topology of the rectifier-inverter system in the input to the motor model.

It is very important to decouple the various stages of a large drive system with the help of B-statements. This eliminates the interaction of the various stages leading to complex non-linear relationships. The decoupled stages undergo local simulation thus reducing simulation run times. With more and more decoupling, larger number of nodes in the circuit are connected to ground, thus forming a sparse matrix during simulation.

For a large complex circuit simulation as in the present case, a functional model for some parts of the circuit produces a dramatic simplification of the drive system. On the other hand accurate modeling of complex converter circuits may lead to a very large number of devices and components and the simulation becomes very time consuming. The same applies when increasing the switching frequency and the simulation run interval. The probability of encountering convergence problems also increases with the number of components and non-linear devices.

7.3.2 Waveform and analysis of 12-pulse, 3-level PWM VSI Drive

SPICE3 simulation waveforms for the 12-pulse, 3-level PWM VSI Drive are shown in Fig.7.5. Fig.7.5(a) shows the corresponding primary voltages of the d and q equivalent circuit and are 90° phase shifted to each other thus validating the d-q axis model of the transformer. The secondary phase voltages and line-line voltages of the Δ-Δ, Δ-Y transformer are phase shifted at 30°, see Fig.7.5(b) and Fig. 7.5(c) respectively. The total input line current has a step shape and has significant commutation overlap due to the large magnetizing inductor of the transformer, see Fig.7.6(a). The two series connected diode bridge rectifier give a 12-pulse rectified output, see Fig.7.6(b). Fig. 7.6 (c) shows the input line currents to the rectifier. The input and output currents of the Δ-Δ transformer are in phase with each other.

Fig.7.6(d) shows the characteristic inverter input dc link current. The chopped nature of the dc link current is due to the pulse width modulation of the inverter.

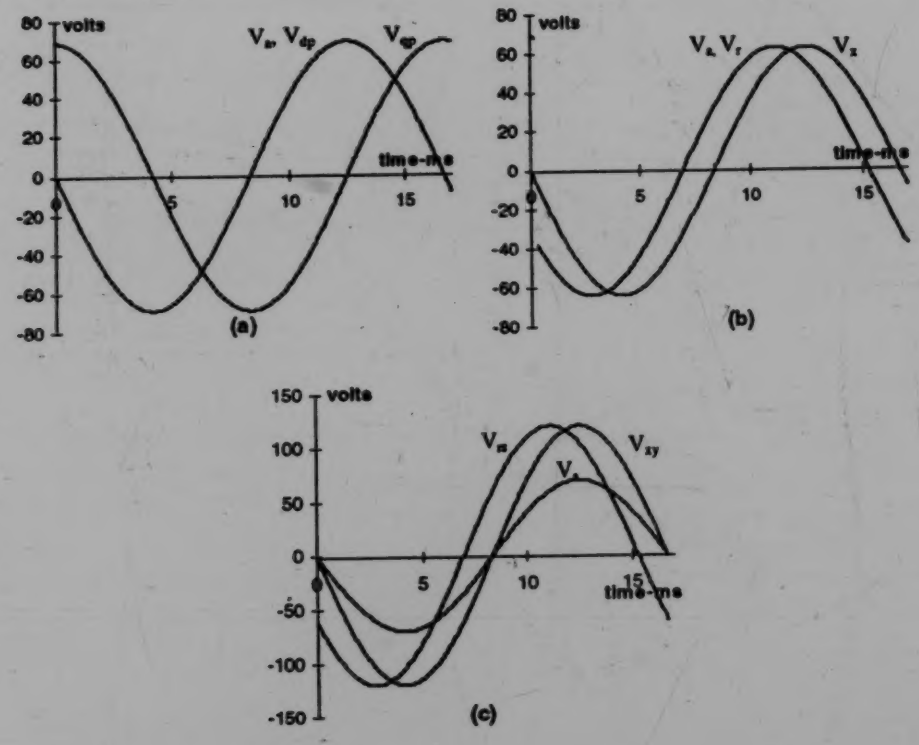


Fig. 7.5 Simulated waveforms for 12-pulse, 3-level PWM Inverter drive, (a) d and q equivalent circuit primary voltages, (b) Δ-Δ, Δ-Y transformer output phase voltages, (c) Δ-Δ, Δ-Y transformer output line-line voltages.

The voltage across the split capacitors is fed to the 3-level inverter with the help of the B-statements. The output terminal potential varies between +E/2 and 0 or -E/2 and 0, see Fig.7.8(a). The phase voltage of the inverter in Fig. 7.8(c) has the three-level waveshape.

Fig.7.9 shows the operation of the inverter drive for a constant volts per hertz. Separate simulation runs are performed for 60Hz, 40Hz and 20Hz by varying the frequency and magnitude of the reference sinusoidal voltage proportionally to keep V/f

V/f constant. In this way the speed can be controlled by adjusting the frequency, keeping the air-gap flux constant by varying the voltage magnitude in a linear proportion to the frequency.

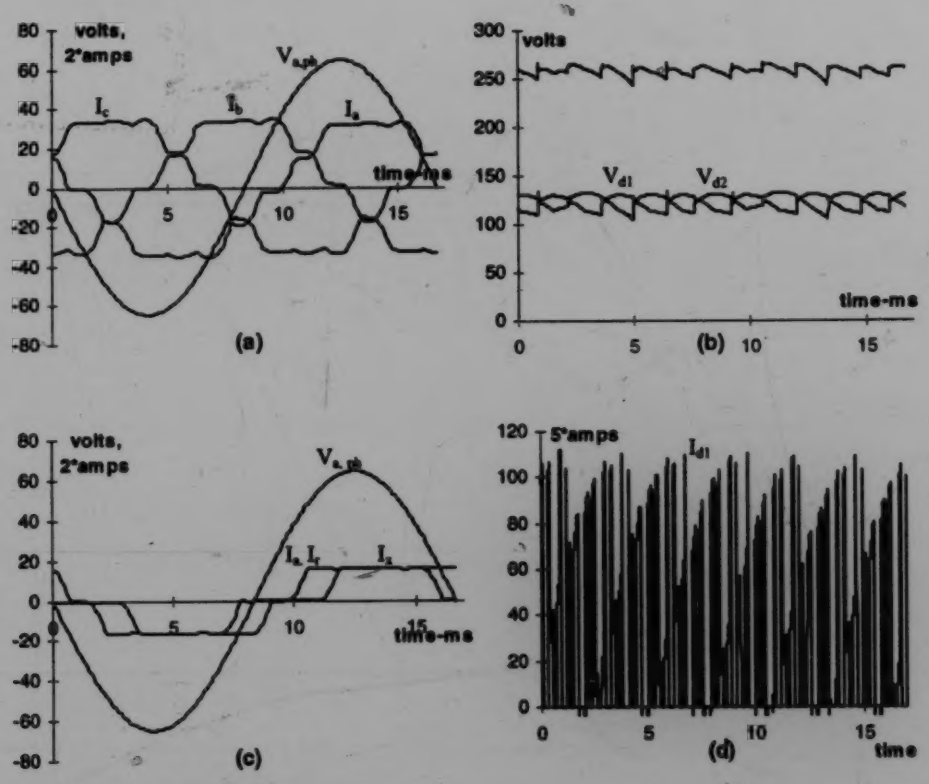


Fig. 7.6 Simulated waveforms for 12-pulse, 3-level PWM Inverter drive, (a) 3-phase total input line currents and phase a voltage, (b) 6-pulse and 12-pulse rectified output voltages, (c) rectifier input line current and phase a voltage, (d) dc-link current.

Fig. 7.7 shows the simulated waveforms for the three-level pulse-width modulation. A sinusoidal reference wave is compared with a triangular carrier wave to generate the PWM pattern.

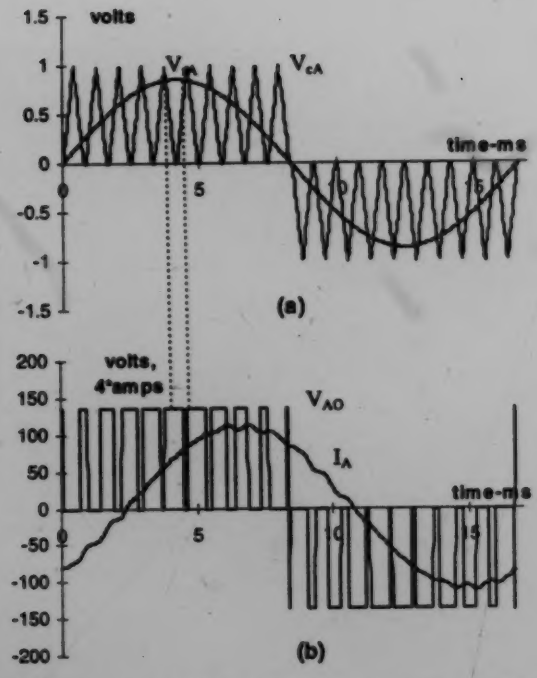
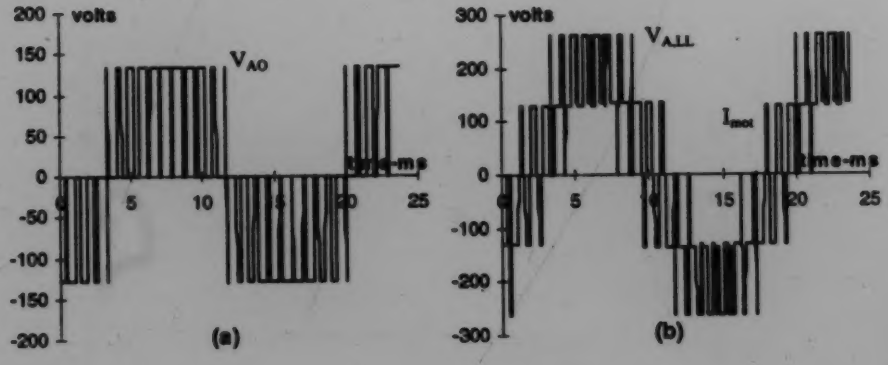


Fig. 7.7 Simulated switching pattern waveforms, (a) Reference and Carrier waves, (b) phase to neutral voltage and line current.



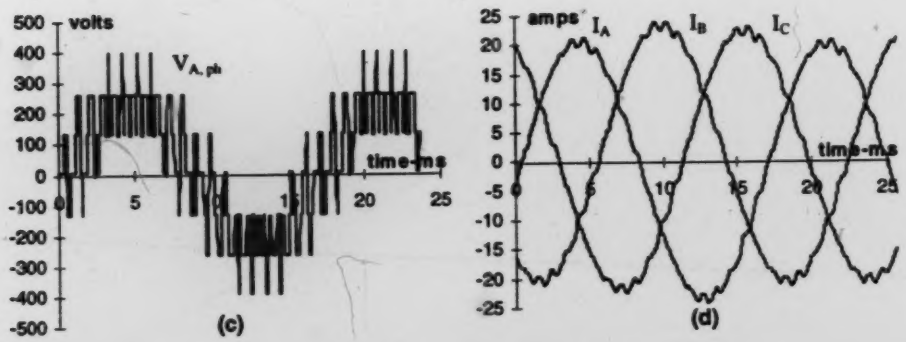


Fig. 7.8 Simulated waveforms for 12-pulse, 3-level PWM Inverter drive, (a) phase to neutral voltage, (b) line-line voltage, (c) phase voltage, (d) line currents.

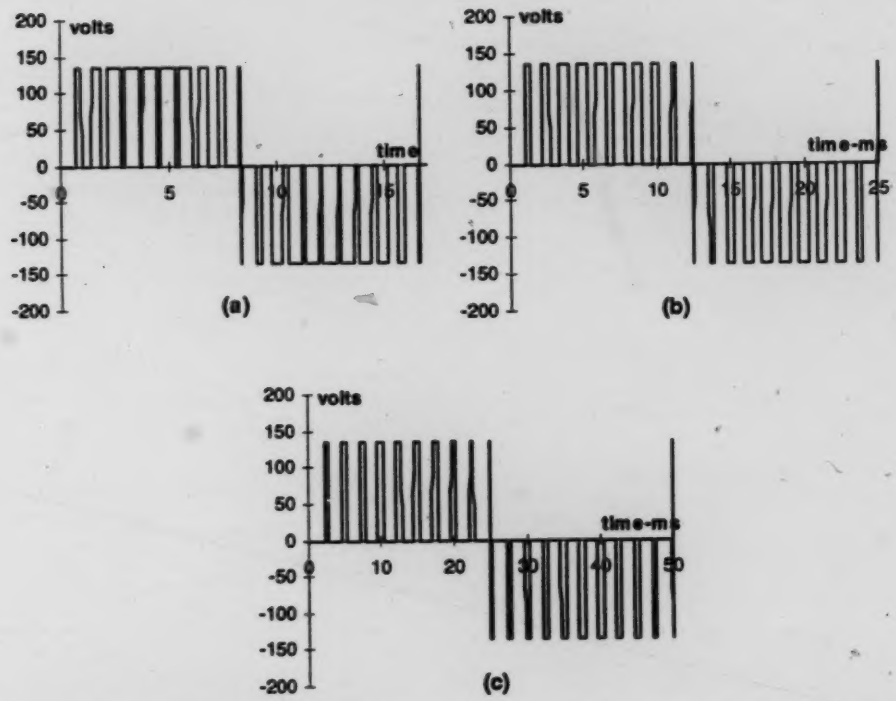


Fig. 7.9 Simulated waveforms for constant volts per hertz operation of 12-pulse, 3-level PWM Inverter drive, (a) 60Hz, (b) 40Hz, (c) 20Hz.

7.4 VSI and CSI Drives

Because of the large value of dc link inductor, the dynamic response of a CSI drive is slower compared to a PWM VSI drive. Because of the large filter capacitor, the dynamic response of a six-step VSI drive is nearly as slow as that of a CSI drive. In the case of VSI drives, the use of PWM allows efficient and smooth operation, free from torque pulsations and cogging [4]. Because of the low frequency of operation of a CSI, PWM is possible only at low speeds. This eliminates torque pulsations at low speeds but not at high speeds. When the source is dc, a PWM VSI drive will be much cheaper compared to a CSI drive of the same rating. Because of the large commutation capacitors and large dc link inductor, which is oversized to prevent saturation, the volume and weight of a CSI drive is much larger compared to a PWM VSI drive.

The use of voltage and current functions to decouple various parts of the circuit, simplifies approach to drive simulation and prevents the interaction between the power-electronic circuits and the drive motor. Most of the digital computer simulation is based on the formulation of a set of system equations, which are subsequently programmed in a high level language. The resultant "equation-based" drive simulation is usually customized for one particular drive systems. SPICE3 on the other hand offers user interactivity since component changes can be made with relative ease and the effects of these on performance quickly assessed. This feature becomes particularly important for simulation of large drive topologies.

Chapter 8

NOVEL RECTIFIER TOPOLOGY

The application of naturally commutated converters in industrial variable speed drive systems has increased over the years to a point where the converter now forms a significant fraction of the load on a utility system [39]. Six-pulse and twelve-pulse uncontrolled diode bridges are commonly used as an interface between the three phase electric utility and power electronic loads. Large harmonics, poor power factor and high total harmonic distortion (THD) in the utility interface are common problems when nonlinear loads such as adjustable speed drives, power supplies, UPS systems, etc. are connected to the electric utility. In this chapter a novel rectifier topology is presented that lower the line current THD with a power factor close to unity. The rectifier performance is assessed with emphasis to its power factor, the per-unit inductor size and the line current total harmonics distortion (THD). The use of SPICE3 simulation tools to obtain the performance factors and design curves of the new rectifier topology is explained.

8.1 Current harmonics and power factor

All power electronic converters can add to the inherent power line disturbance by distorting the utility waveform due to the harmonics injected into the utility grid and by producing electromagnetic interference. A simple block diagram of the utility interface is given in Fig.8.1. The line current i_s, can be considered to be the sum of the fundamental component i_1, and the other harmonic components i_h. Due to the finite internal impedance of the utility source which is simply represented by L_s in Fig.8.1, the voltage waveform at the point of common coupling to the other loads become distorted, which may cause them to malfunction.

Some common effects due to harmonics are

Supply harmonic Currents cause :

Heating in current carrying transformers, capacitors, cables, etc.

Reduction in power factor

Decrease in equipment life span

Telephone interference

Load Harmonic Current Cause :

EMI / RFI emissions

Inverter bridge losses / heating

Motor torque pulsation

Motor winding vibration

Audible noise

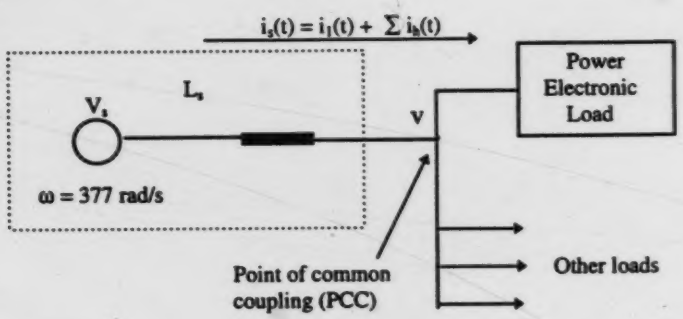


Fig. 8.1 Utility Interface

The power factor PF at which an equipment operates is the product of the current ratio I_1 / I_s and the displacement power factor DPF :

$$PF = \frac{\text{Power}}{\text{Volt-amps}} = \frac{I_1}{I_s} \cdot DPF \qquad (8.1)$$

The displacement power factor equals the cosine of the angle φ_1 by which the fundamental frequency component in the current waveform is displaced with respect

to the input voltage waveform. The current ratio in Eq.(8.1) is the ratio of the rms value of the fundamental frequency current component to the rms value of the total current. The power factor indicates how effectively the equipment draws power from the utility; at a low power factor of operation for a given voltage and power level, the current drawn by the equipment will be large, thus requiring increased volt-ampere rating of the utility equipment. Thus for high power factor operation, the displacement power factor DPF should be high in Eq.8.1. Also the current harmonics should be low to yield a high current ratio I_1 / I_s.

A number of methods have been proposed to overcome the problem of reducing harmonic distortion associated with rectifier circuits at the utility interface [32],[41],[42].

8.2 Rectifier topology

In the present rectifier topology, resonant harmonic correction networks are presented that lower the total harmonic distortion of the input current of the three-phase diode bridge rectifier. The basic harmonic correction network consists of inductors connected in series with the rectifier input terminals and capacitors connected either in delta or star configuration at the input of the rectifiers. This rectifier operates by essentially time multiplexing a resonant current pulse into the ac supply and the resonant action is closely linked to the diode rectification process.

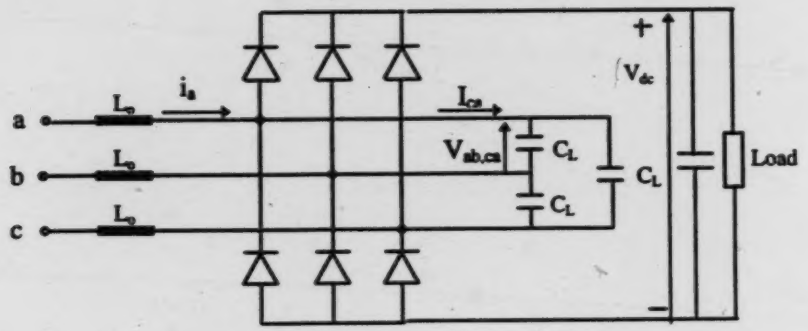


Fig. 8.2 Resonant mode harmonic correction circuit for a 3-ϕ diode bridge

As can be seen from Fig.8.2 the capacitors are connected in a delta connection. Alternatively the capacitor can also be connected in a Y connection and the resonant action remains the same. The delta connection lowers the capacitor size but increases their rms voltage ratings. A high performance can be obtained under the peak load conditions but relatively large per-unit line inductors are required. These characteristics make the rectifier suitable for constant power loads and high frequency ac power sources.

The resonant rectifier described above can be implemented in a 12-pulse rectifier using a Δ-Δ, Δ-Y input transformer as seen in Fig.8.3. The THD obtained by 6-pulse rectifier can be further improved since the Δ-Δ, Δ-Y connection of the input transformer further eliminates the 5^{th} and 7^{th} harmonics [6] as discussed in section 3.3.

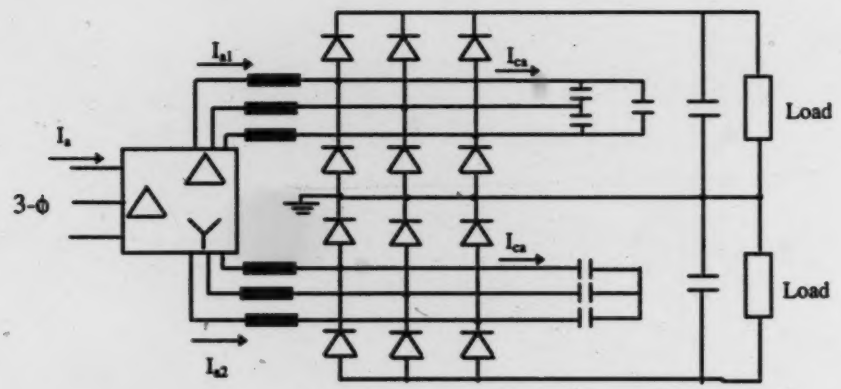


Fig. 8.3. 12-pulse rectifier with a resonant-mode harmonic correction topology.

8.2.1 Simulation of Rectifier topology

The SPICE3 schematic with its corresponding netlist for the 12-pulse rectifier is given in Appendix G.8. One of the diode bridges has the resonant network with delta connected capacitors while the other has a Y connected capacitor. Both are seen to have the same functionality.

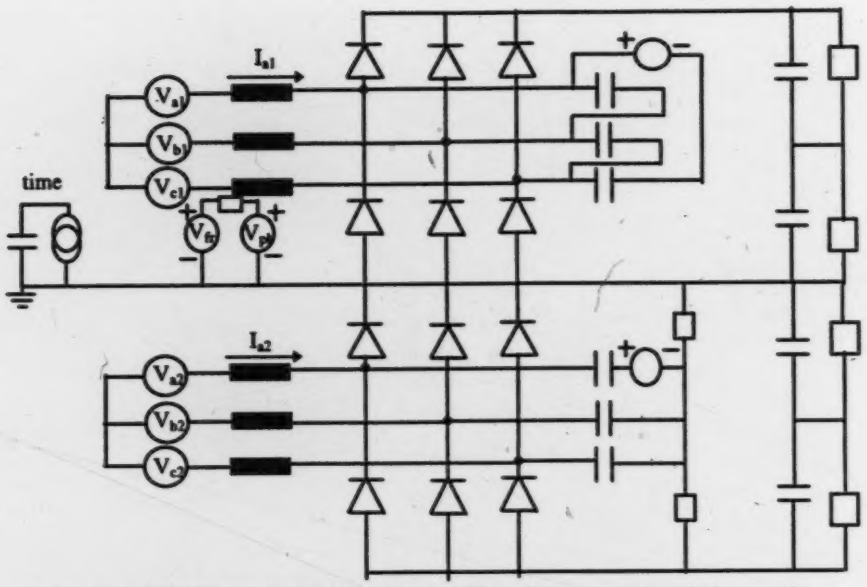


Fig. 8.4 SPICE3 model for 12-pulse rectifier with resonant mode harmonic correction circuit.

The diode model used in the simulation is as follows

.MODEL PD D(IS=1E-15 BV=1200 CJO=1PF TT=0)

The diode is modeled specifying parameters that significantly affect power converter output such as inverse saturation current (IS), reverse breakdown voltage (BV), zero-bias junction capacitance (CJO) and transit-time (TT). The typical values for the diode parameters are taken from the data sheet of a diode IR-type R18C [46]. The dc characteristics of the diode are determined by the saturation current value. Transit time helps in modeling the charge storage effect. The nonlinear depletion layer capacitance is determined by the parameter junction capacitance.

The input to the 12-pulse bridge are the three phase voltages V_{a1}, V_{b1}, V_{c1} and V_{a2}, V_{b2}, V_{c2} which are phase shifted by 30° from each other. Voltage source of zero magnitude are used to sense the current in the delta capacitor networks and also the current flowing through the diode. Resistance are added in the resonant network of

the lower bridge to eliminate the problems of convergence during simulation. These resistors are chosen to be of high value so that very negligible dc link current flow through them thus altering the potential of the Y-connected point.

8.2.2 Waveform and analysis of Rectifier topology

Typical simulated and experimental waveforms are shown in Fig.8.5-Fig.8.8. The SPICE3 model uses the same values for the passive components as are used in the experimental setup. Measurements are made for a 7kW load and 202 V ac supply. The line inductor value is 7.5mH. The resonant capacitor values used in the simulation is 34 μF, though the ones in the experimental setup were a close 33 μF.

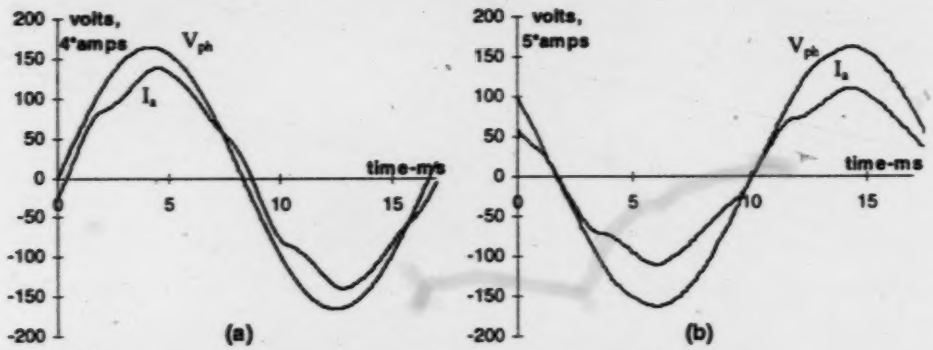


Fig. 8.5 Waveforms for phase voltage (V_{ph}) and line current (I_a) for a 6-pulse rectifier bridge with resonant network, (a) simulated and (b)experimental.

Fig.8.6.(a),(b) show the current through the diode associated with the normal rectification of a 6-pulse diode bridge. The notches in the diode current are due to the input line inductors. The resonant capacitor network draws a resonant current pulse prior to building of the current due to the conduction of the diodes. This is shown in Fig.8.6.(c),(d). The resultant line current has a low distortion and almost unity power as seen in Fig.8.5(a),(b).

Fig.8.7(a) and (b) show the voltage across the capacitor of the resonant network and the line-to-neutral voltage. As seen from Fig.8.7(d) each capacitor charges up to the dc rail voltage and a resonant current pulse builds up during the charging period. Thus each capacitor contributes two resonant pulses in each half

cycle, see Fig.8.7(c). Referring to the simulation waveforms of Fig.8.6(a) and Fig.8.7(c) we see that at the zero time instant the capacitor across line a-b is at $-V_{dc}$. The capacitor starts discharging to zero volts and a current pulse I_{ca} is drawn from the utility. During this period there is no current flow through the diode i.e $I_{da} = 0$. This

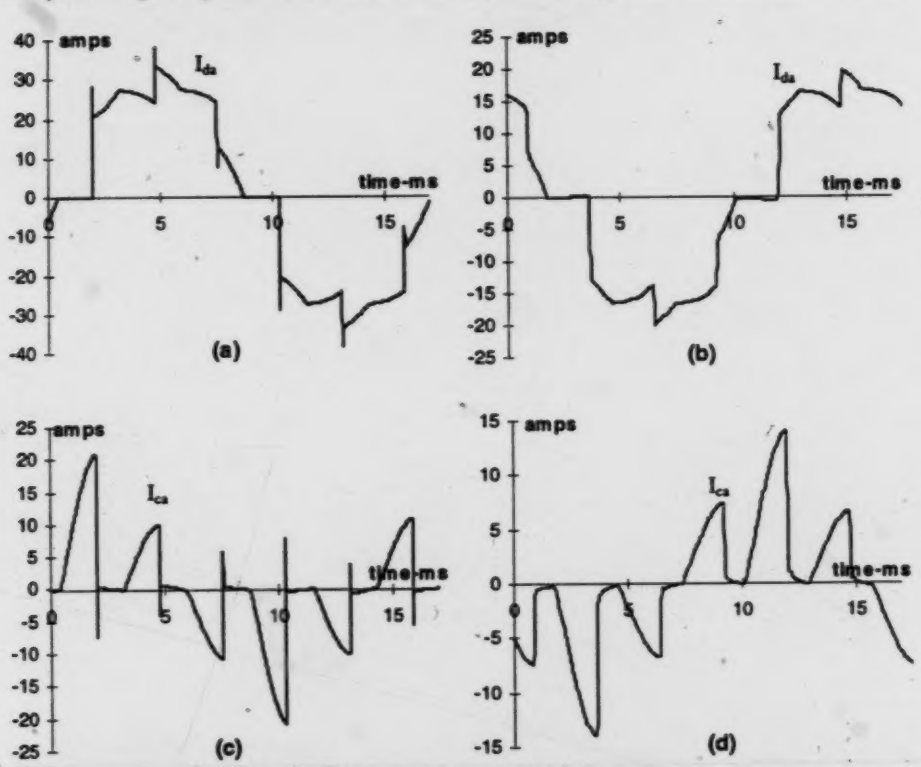


Fig. 8.6 Simulated and experimental waveforms for 3-phase diode bridge with resonant network, (a) simulated diode current (I_a -I_{ca}), (b) experimental diode current (I_a -I_{ca}), (c) simulated capacitor current (I_{ca}), (d) experimental capacitor current (I_{ca}).

resonant pulse thus helps to waveshape the phase a line current. The capacitor then charges to $+V_{dc}$ and another current pulse is drawn by the same capacitor that help is waveshaping the line current of another phase.

Fig.8.9 show the 6-pulse output rectifier voltage with minimal ripple due to the capacitor dc-link, with the value close to 272.2V (1.35x202). This is highly desirable for high power application.

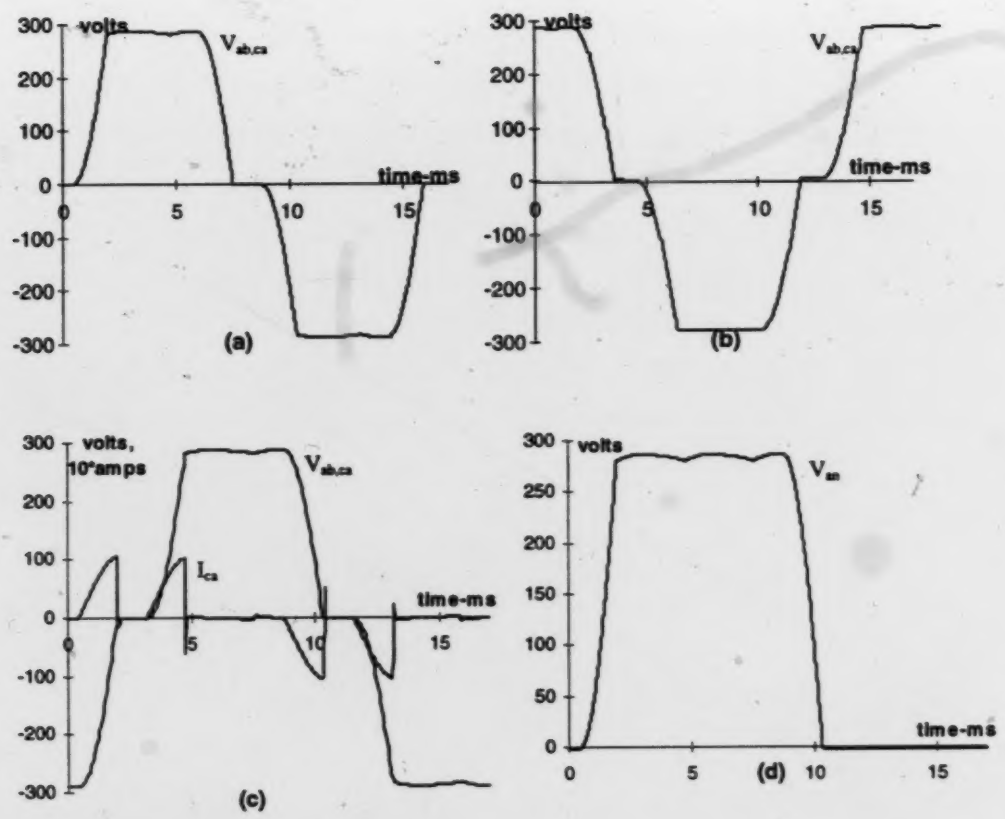


Fig. 8.7 Waveforms for the resonant capacitors, (a) simulated voltage across capacitor, (b) experimental voltage across capacitor, (c) simulated phase a to neutral volatge, (d) simulated capacitor voltage and resonant pulses.

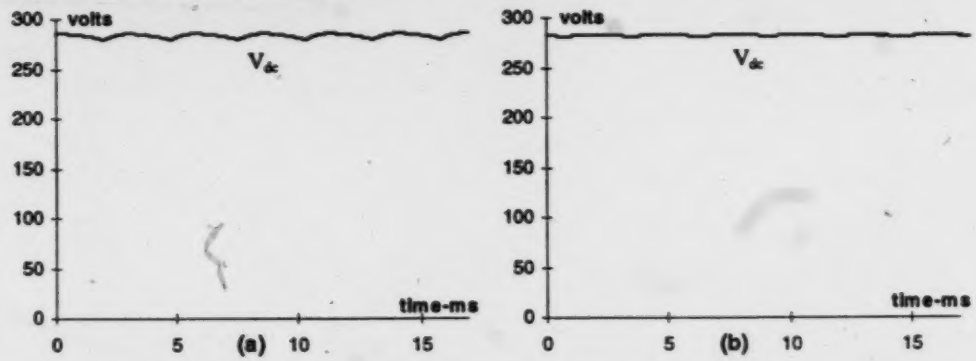


Fig. 8.8 Simulated and experimental waveforms for the 6-pulse output rectifier dc voltage

Harmonic analysis of the resonant network is done using both SPICE3 and experimental data and is given in Appendix F. As seen from the SPICE3 simulation results, a low THD of 6.1 % and 8.6 % are obtained for the upper and lower 6-pulse diode bridges. The line current is nearly sinusoidal with unity power factor. This is a significant improvement over the 6-pulse diode bridge with LC filter which gave a THD of 27.6 % at 0.96 PF as discussed in Chapter 3. The total line current of the 12-pulse bridge has a THD as low as 3.3 % with a power factor of 0.97. This THD is much better then the THD of 7.3 % obtained for a 12-pulse rectifier without the resonant network as discussed in Chapter 3. The significant improvement in the THD for a 12-pulse rectifier is due to the cancellation of the 5^{th} and 7^{th} harmonics as can be seen from the harmonic analysis in Appendix F.

8.2.2 Simulation tools used for circuit Performance Analysis

SPICE3 consists of a front end for data analysis and plotting. This is the Interactive Interpreter and can be run as a separate "stand alone" program. This run file is executed in batch mode using it as a raw file with the "-b" option. The general format of the program used for the design analysis is given below.

```
scr resonant circuit
.controlc
set width = 275; set nobreak; set noheader; set noprintscale
source netlist file
let name = expression;
.....
.....

    while condition
        .....
        .....
        alter device value;
        .....
        .....
        tran tstep tstop tstart tmax uic
        let name = expression;
        .....
```

```
            .....
            destroy all
        end
print col expression ... >> output file
.endc
.end
```

The script begins with a blank line or a simple text line which is not read during execution time. This is followed by the .CONTROLC statement. All SPICE3 commands are enclosed between the .CONTROLC statement and the .ENDC statement. These commands are executed immediately after the circuit is loaded.

To generate the data for post processing the **set** options are fixed for the plot width with no headers and no page breaks. The netlist file is sourced once at the beginning of the program. To start with, all the new vector are initialized to a value specified by the expression using the **let** command.

The **while-end**, uses an arbitrary condition which may be in the form of a algebraic expression, which if true, executes the statement within the while-end loop. The values for the various vectors are changed within the while loop using the **alter** command. Each command is separated from the other by a semi-colon. The **let** command is used in the while loop to set up the equations for the various performance curves.

The **tran** statement performs a transient analysis and the time-step of simulation is adjusted to obtain smoother and accurate curves. At the end of each loop the data generated is destroyed using the command **destroy.** This helps in memory management and performs the simulation in each loop afresh since it releases the memory holding the data for the specified run. The various vectors calculated for the performance curves are printed in column format to a file using the **print** command. The ">>" is used to direct the data to an *output file* in the append mode since the data is dumped to the file after every loop. The program finally ends with the **.end** statement.

8.2.3 Performance Analysis and Design

The analysis of the rectifier topology was achieved using .controlc statement, see Appendix G and choosing a constant 7kW power level, with a 202 V, 60Hz ac supply. All performances are plotted in per unit values relative to the rectifier ratings and so can be applied to any rectifier rating. The relationship between the magnitudes of the capacitors connected in Δ (C_L) and in Y (C_o) connection is given as follows:

$$C_o = 3\,C_L \tag{8.2}$$

The resonant circuit parameters are defined as follows :

$$\omega_o = \frac{1}{\sqrt{LoCo}},\quad f_o = \frac{1}{2\pi\sqrt{LoCo}},\quad Z_o = \frac{\sqrt{Lo}}{\sqrt{Co}} \tag{8.3}$$

With these definitions, the performance of the rectifier topology is analyzed by keeping ω_o constant and varying Z_0 and vice-versa. Fig.8.10 and Fig.8.11 show the performance curves for varying Z_0 and ω_o respectively. It has been seen that lowering the time step for SPICE3 simulation gives much accurate results and smoother curves. Also the analysis is done for a significant long duration of 350ms for the simulation to settle down.

The THD results in Fig.8.10(a),(c) show that the 6-pulse rectifier achieves a low line current distortion at the expense of a low power factor. Current distortion levels of between 7 to 15% can easily be achieved. The line current THD for the 12-pulse rectifier as shown in Fig.8.10(b) has a significant improvement and can very easily achieve levels under 5% with reasonable per-unit line inductors, 0.1 or 0.2 p.u. The rectifier power factor peaks at Z_0 = 1.5 p.u for both 6-pulse and 12-pulse rectifier, Fig.8.11(a),(b). Fig.8.11(c),(d) show similar trend in the fundamental power factor angle for both 6-pulse and 12-pulse and follow the general trend of the corresponding power factor curves. Fig.8.10(c),(d) show the change in THD with PF. For each curve the power factor peaks for a certain THD and this defines the desirable operating point for the circuit.. The curves illustrate that the lowest resonant

frequency achieves the lowest line current distortion at the highest power factor. A desirable value for Z_o lies between 3 and 5 for a fairly low THD.

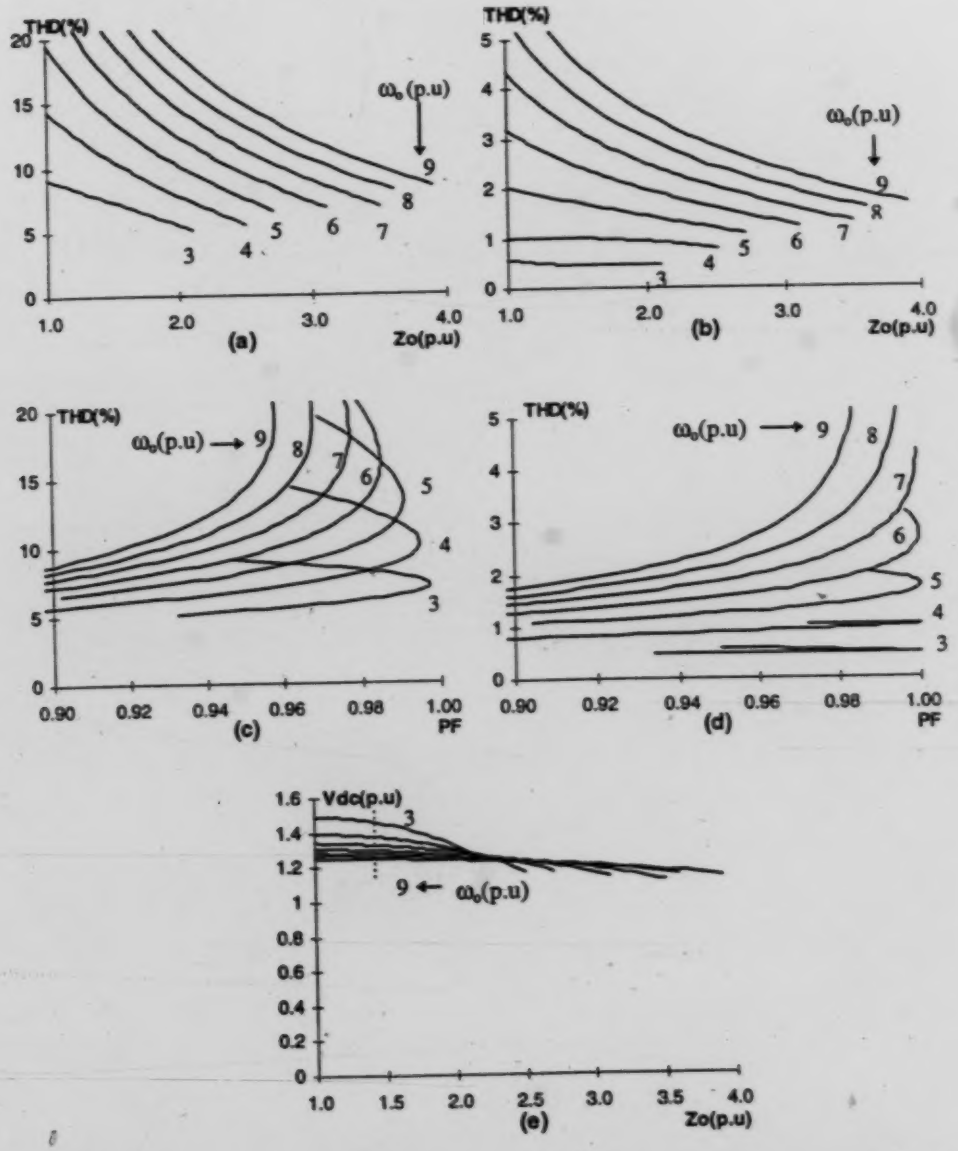


Fig. 8.9. 6-pulse and 12-pulse rectifier performance curves keeping ω_o constant and varying Z_o, (a) line current total harmonic distortion (6-pulse), (b) line current total harmonic distortion (12-pulse), (c) line current THD Vs power factor (6-pulse), (d) line current THD Vs power factor (12-pulse), (e) dc link voltage (V_{LL} = 202V)

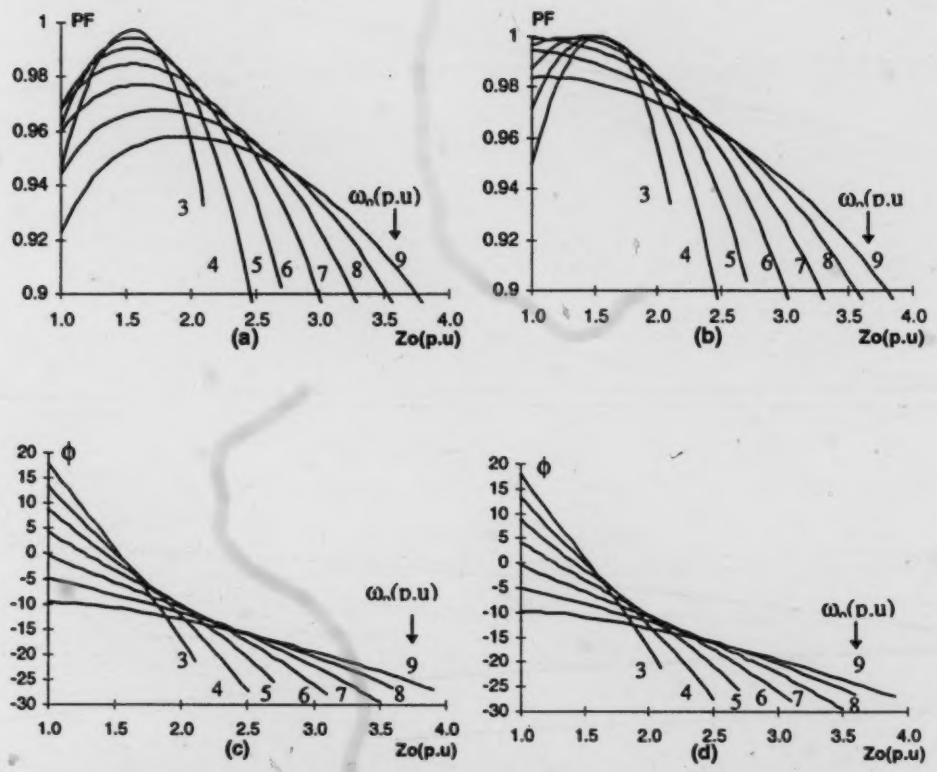


Fig. 8.10. 6-pulse and 12-pulse rectifier performance curves keeping w_o constant and varying Z_o, (a) power factor (6-pulse), (b) power factor (12-pulse), (c) fundamental power factor angle (6-pulse), (d) fundamental power factor angle (12-pulse)

Similar curves are shown in Fig.8.12 and Fig.8.13 where the rectifier performance is obtained as Z_o is changed keeping ω_o fixed. Fig.8.12(a) shows that the line current distortion decreases as the resonant frequency is decreased. For a 12-pulse rectifier THD as below 3% is easily achieved for larger values of Z_o, as seen in Fig.8.12(b). Fig.8.13(a), (b) shows that the power factor decreases rapidly as ω_o is decreased. Power factor improves for lower values of Z_o. Consistent with the trend in Fig.8.11(a),(b), unity power factor is achieved for Z_o value of 1.5. Fig.8.12(e) shows that the dc-link voltage collapses as ω_o is decreased to a low value. Both these trends are consistent with the line inductance becoming too large. The rectifier THD variation with PF is seen in Fig.8.12(c), (d). The curves illustrate that the THD at the

peak power factor is reduced as ω_o is lowered. A desirable ω_o lies between 2.5 and 1.5.

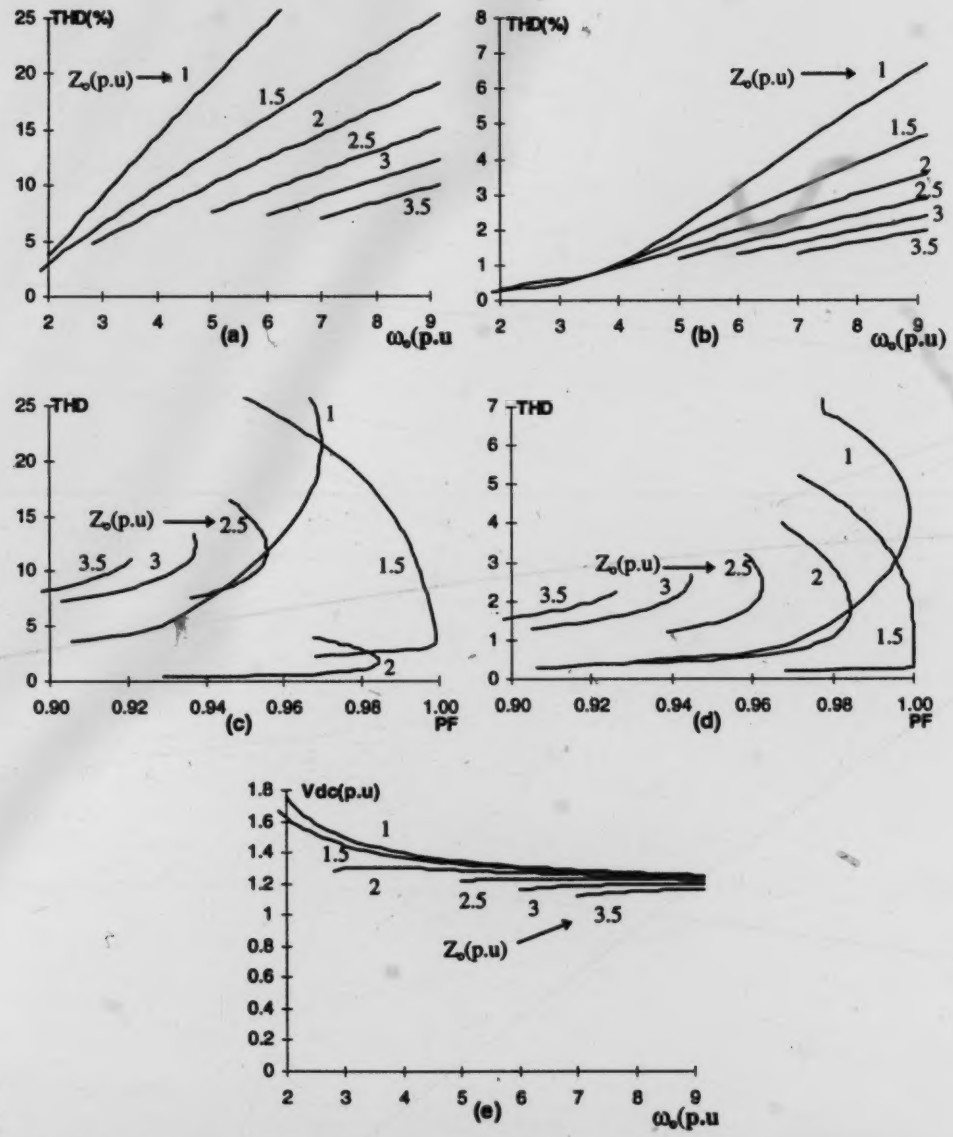


Fig. 8.11 6-pulse and 12-pulse rectifier performance curves keeping Z_o constant and varying ω_o, (a) line current total harmonic distortion (6-pulse), (b) line current total harmonic distortion (12-pulse), (c) line current THD Vs PF (6-pulse), (d) line current THD Vs PF (12-pulse), (e) dc link voltage (V_{LL} = 202V)

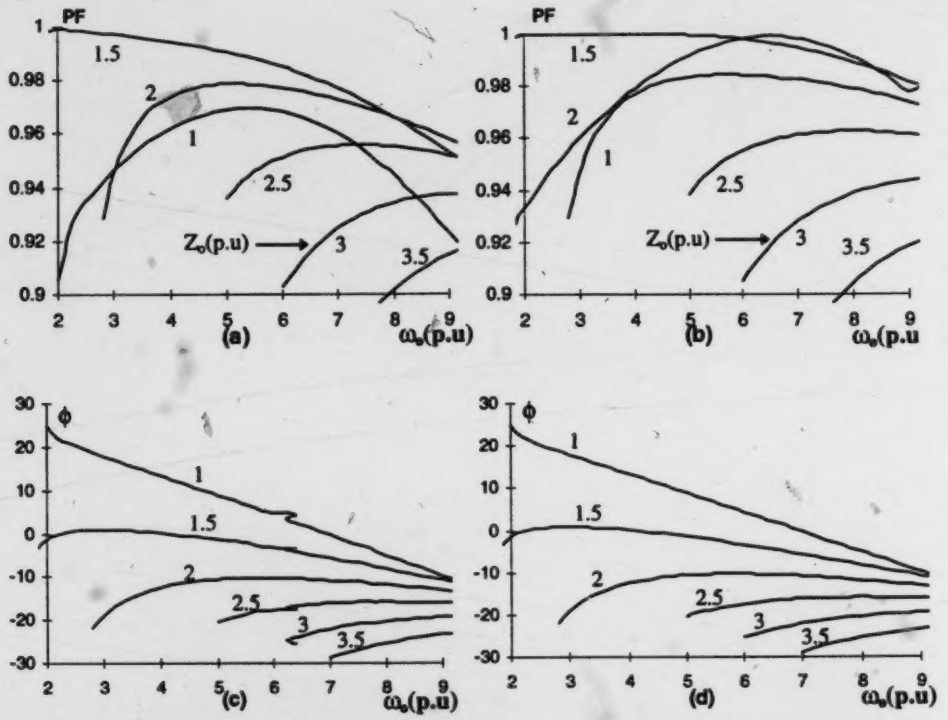


Fig. 8.12 6-pulse and 12-pulse rectifier performance curves keeping Z_o constant and varying ω_o, (a) power factor (6-pulse), (b) power factor (12-pulse), (c) fundamental power factor angle (6-pulse), (d) fundamental power factor angle (12-pulse).

The SPICE3 simulation tools thus effectively help in analyzing a new rectifier topology. The performance curves identifies the trade-off between the total current harmonic distortion and power factor. Its helps in deciding the most optimal and cost effective point of the circuit operation. The dc-link voltage is seen to collapse for larger values of the inductance, so that a limit needs to be set for the inductor value.

The resonant harmonic correction technique suffers from a variable power factor and high distortion at low power levels. In particular, under light loads, a leading power factor is obtained with high current distortion and erratic operation. These problems can be reduced using thyristor networks to control the position of the resonant pulse drawn in advance of the normal diode conduction periods. The thyristors can guarantee that the resonant action does not start until after the zero

voltage cross-over of the line-to-neutral voltage. Additional benefits are obtained in decoupling the resonant action from the ac utility supply.

The novel rectifier topology helps in obtaining a low input line THD with nearly sinusoidal line current at unity power factor thus complying with the limits specified in IEEE-519 [47] and proposed by the IEC-555 [48]. The additional advantages of the proposed topology are as follows :

- The proposed scheme is passive and does not interfere with the ac to dc rectification process of the diode rectifier topology.
- The required VA rating of the passive components is a fraction of the diode rectifier VA.
- These topologies do not use high frequency switches, thus reducing the switching losses and are well suited for industrial applications.
- The resonant network draws negligible fundamental current from the input supply.
- The proposed scheme can be viewed as a cost effective retrofit to the existing wide range of diode rectifier type utility interface applications.

Chapter 9

CONCLUSIONS

This work presents various simulation techniques, implemented using SPICE3 for simulating Power Electronic systems. The study of new control strategies, the effect of harmonics and the performance analysis of the system are facilitated by simulation results. The comparison of simulation results with experimental ones validate the simulation techniques of the drive topologies. A novel rectifier topology is presented that draws line current from the utility with low current distortion and unity power factor.

9.1 SPICE3 Simulation

The more recent version of SPICE3, namely .3f4 has various advanced features that are very useful for implementing improved models and system analysis of power electronic simulation and analysis [1]. The SPICE3 B-statement and U-statement has simplified the structure of control and switching function. SPICE3 also provides an Interactive Interpreter that can be used as a stand alone program in the form of a .CONTROL file. This feature of SPICE3 has been used in this work for design and performance analysis of Power Electronic circuits.

The understanding of SPICE3 as a continuous time driven simulator is very helpful in obtaining quick solutions to simulation problems. The most frequently occurring error in the simulation is due to the inability for the matrix solution to converge. The initial time step chosen as the initial guess for convergence is very important for the matrix solution.

In the present work, a large number of power electronic circuits with varying complexity have been simulated. Simulation run time increases with the increase in the number of nodes and switches. Most of the circuits use a diode that take considerable less time then if a BJT or MOSFET was used. A better diode model can

be used by choosing the various device parameters from the manufacturers data handbook. This model is used in the novel rectifier topology, where the device parameters are adjusted to get better convergence during simulation.

The timely construction of performance curves of the novel rectifier topology, helps the results to be obtained at the least time step possible. Choosing a small time step for transient analysis also increases the resolution of the simulated waveforms obtained and prove a better aid for analysis than the experimental waveforms whose resolution is restricted by the resolution of the oscilloscope. This feature of SPICE is seen particularly for PWM inverter topologies where a high switching frequency is used.

Simple representation of various circuits is achieved by decoupling the complex circuitry so that they can be simulated as independent block of circuits. For instance, the output of the transformer is decoupled from the input of the rectifier in the 12-pulse rectifier topology with the help of B-function. This kind of modeling isolates the two circuitry and simplifies simulation. Decoupling various parts of the circuits connects more number of nodes to ground so that a much sparse nodal admittance matrix is obtained. Sparse Matrix technique is used instead for matrix solution thus increasing the speed of simulation.

Data for the various simulation waveforms are generated using the netlist file as a raw file. Similarly the data for the experimental waveforms are generated using the data acquisition system, LABVIEW. Experimental results are used to verify the simulations. SPICE3 has the provision of doing harmonic analysis for the various currents and voltages with the help of the .controlc functions. Comparison of the simulated analysis with experimental ones show close agreement.

9.2 Drive Topology

The two drive topologies discussed in this work are the Voltage Source Inverter and Current Source Inverter. The input, output and load of the drive systems are simulated and analyzed separately before simulating the complete drive system.

Rectifier:

The rectifier stage have either a 6-pulse or a 12-pulse operation. For the input to a 12-pulse rectifier stage to both the drive topology we use a Δ-Δ, Δ-Y transformer that is highly applicable for high power. The 30° phase shift between the secondaries of the two transformer cancel the 5^{th} and 7^{th} harmonics in the input line current thus significantly improving the total current distortion. The series connection of two diode bridges form a 12-pulse rectifier. The THD of this 12-pulse rectifier which is a low 7.3 % at a power factor of 0.98 as compared to a 6-pulse diode bridge rectifier with C-filter with THD of 68.7 % at power factor of 0.81 and 6-pulse diode bridge rectifier with LC-filter with THD of 27.6% with power factor of 0.96. The 12-pulse rectifier has the 11^{th}, 13^{th}, 23^{rd} and other higher order harmonics in the input line current which make filtering relatively easy as compared to 6-pulse operation.

Δ-Δ, Δ-Y transformer:

The modeling of the Δ-Δ, Δ-Y transformer is achieved using d-q axis theory. Functions can be used to decouple the d-q axis model of the Δ-Δ, Δ-Y transformer from the inputs of the rectifier. The value of the transformer d-q axis parameters can be directly linked to experimentally measured parameters and this is very helpful in the comparison of the simulation and experimental results.

Voltage Source Inverter:

The dc link for the VSI is a capacitor that keep the input voltage to the inverter stage constant. Both square wave inverter and PWM inverter is considered in this work. The square wave inverter requires a phase controlled rectifier input stage for controlling the input dc voltage. The phase controlled rectifier is simulated by modeling the thyristor as a switching device. The pulse width modulation of the voltage source inverter reduces the harmonics in the output line voltage, so that the THD of the line voltage reduces to 17% in a PWM VSI from about 24% for a square wave VSI. A generalized structure of a three-level voltage source inverter is described. The simulation waveforms of the three-level inverter show close

resemblance with theoretical results. It also reduces the significant 5^{th} and 7^{th} harmonics.

Current Source Inverter:

The dc link for the CSI is a large inductor that helps to keep a stiff input current to the inverter. Modeling of a PWM CSI is discussed in this work. Capacitors are connected at the output of the inverter to absorb high frequency harmonics associated with the pwm inverter output current. As a result the THD of the motor line current improves significantly to 2.3 % from that of the CSI line current THD of 8.8%. The inverter legs are modeled as three pwm current functions that simulate the switching action of the six switching devices. This allows less run time during SPICE3 simulation due to lesser number of switching devices.

Induction Motor :

The induction motor is used as the load to the inverter stage. The induction motor is modeled using d-q axis theory in very much the same manner as the transformer. Transformation of the a-b-c axes to the d-q axes eliminates the time-varying parameters making modeling much simpler. The availability of the B-statement and the U-statement in SPICE3 facilitate the modeling of the complex equations, see paper in Appendix H. The model parameters are the same as that of the actual machine obtained from various tests, see Appendix D. The simulation results show good agreement with the corresponding experimental results, thus confirming the validity and accuracy of the motor model.

Constant V/f operation for the induction motor is explained. The existing model of the motor is modified to obtain simulation results at steady state for a fixed speed. The .CONTROL statement in the command interpreter is used to obtain various curves for different values of V/f. The command interpreter which is a new feature of SPICE3 can be used to vary the parameters easily using simple self explanatory syntax.

9.3 Novel Rectifier Topology

The work describes a novel rectifier topology for the 6-pulse and 12-pulse diode bridge rectifiers. These rectifiers use resonant pulses to improve the line current distortion associated with the rectifiers, see paper in Appendix H. The operation of the rectifiers are illustrated with reference to the SPICE3 simulation and experimental results. The performance of the rectifiers are investigated with reference to the line current distortion (THD), rectifier input power factor and size of the line inductors. The analysis is done using performance curves obtained using SPICE3 simulations.

The novel rectifier topology for a 6-pulse diode bridge rectifier gives a low THD of 6.1 % with the line current nearly sinusoidal at unity power factor. This is a significant improvement from the 6-pulse diode bridge rectifier with C dc-link filter with THD of 68.4 % and power factor of 0.81 or a LC dc-link filter with a THD of 27.6 % and power factor of 0.96. The line current quality further improves for the novel 12-pulse rectifier topology and THD of less then 5% is easily obtained. A low line current distortion of 3.3 % at 0.97 power factor is obtained. These proposed topologies can be viewed as a cost effective retrofit to the existing wide range of diode rectifier type utility interface applications.

9.4 Suggestions for Further Work

SPICE3 simulation is highly dependent on the number of switches and nodes used in the circuit model. The rectifier topologies used in this work use a minimum of six switching devices. Thus, a significant improvement in both simulation run time and convergence problem can be achieved by modeling the entire diode bridge as a functional model using a single function statement or at least three function statements representing each leg of the diode bridge.

For the novel rectifier topology all the data for the performance curves are obtained using a time-step of 5 μs. The curves, specially those of the line current THD can be further smoothened by using a smaller time-step. The values of the

relative tolerance and absolute tolerance have to be adjusted accordingly to get a good convergence at such small time-steps.

The proposed rectifier topology gives erratic operation and a leading power factor under light loads. These problems can be overcome by using a thyristor network used as a Y-switch to control the position of the resonant pulse drawn in advance of the normal diode conduction period.

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APPENDIX

A Harmonic analysis data for 6-pulse diode bridge rectifier

C Filter : C=940 μF, R=16.67 Ω

SPICE simulation data

Fourier analysis for i(b13):

No. Harmonics: 10, THD: 68.3614 %, FPF: 0.99, PF: 81%

	Magnitude	Phase
I_1 =	17.782 A	172.744
I_5 =	10.5237 A	10.5237
I_7 =	6.0823 A	114.366

Experimental data

P=4.4 kW, S= 5.7 kVA

Vab= 198 V, THD=84.4 %, PF=.77, FPF=1

Ia = 16.7 A

I_1 = 12.3 A

I_5 = 9.1 A

I_7 = 6.9 A

LC filter : C=940 μF, L=2.5mH, R=16.67 Ω

SPICE simulation data

Fourier analysis for i(b13):

No. Harmonics: 10, THD: 27.6128%, FPF: 0.99, PF: 96.4%

	Magnitude	Phase
I_1 =	18.2155 A	178.525
I_5 =	4.6292 A	-17.837
I_7 =	1.9660 A	36.5576

Experimental data

P=4.15 kW, S= 4.32 kVA

Vab= 198 V, THD=31 %, PF=0.96, FPF=1

Ia = 12.7 A

I_1 = 12.1 A

I_5 = 2.7 A

I_7 = 1.4 A

B Test data for Δ-Δ / Δ-Y transformer parameters

TRANSFORMER NAMEPLATE DATA

KVA = 3 kVA V_{rated} = 208 V I_{rated} = 13 A

OPEN CIRCUIT TEST (at rated voltage)

Δ-Δ transformer

V_1(V)	I_1 (A)	V_2(V)	P_{in} (KW)$_{3phase}$
202.4	1.9	201.5	0.11

R_m = 123 Ω Z_m = 106.5 Ω X_m = 212 Ω L_m= 0.562 H

Δ-Y transformer

V_1(V)	I_1 (A)	V_2(V)	P_{in} (KW)$_{3phase}$
202.4	2.76	201.1	0.14

R_m = 97.53 Ω Z_m = 73.33 Ω X_m = 111 Ω L_m= 0.294 H

SHORT CIRCUIT TEST (at rated current)

Δ-Δ transformer

I_1 (A)	V_1(V)	P_1 (KW)
9.9	12.43	216

R_1 = 0.46 Ω Z_1 = 0.796 Ω X_1 = 0.649 Ω L_1 = 1.7mH

Δ-Y transformer

I_1 (A)	V_1(V)	P_1 (KW)
10.1	12.67	216

R_1 = 0.448 Ω Z_1 = 0.797 Ω X_1 = 0.659 Ω L_1 = 1.74mH

C Harmonic analysis data for 12-pulse diode bridge rectifier

L=2.5mH, R=41.666 Ω

SPICE simulation data

Fourier analysis for i(b13):

No. Harmonics: 10, THD: 7.32 %, FPF: 0.985, PF: 0.982

	Magnitude	Phase
I_1 =	19.864 A	-9.7219
I_5 =	1.2266 A	140.405
I_7 =	0.7618 A	125.005
I_{11} =	1.176 A	
I_{13} =	0.995 A	
I_{23} =	0.56 A	

Experimental data

P=6.3 kW, S= 6.5 kVA

Vab= 194 V, THD=10.9 %, PF=0.97, FPF=0.98

Ia = 19.5 A

I_1 = 19.4 A

I_5 = 0.2 A

I_7 = 0.6 A

I_{11} = 1.6 A

I_{13} = 1.1 A

I_{23} = 0.6 A

D Test data for Induction Motor parameters

MOTOR NAMEPLATE DATA

HP/KW = 7.5 HP Number of poles = 4 $Speed_{(synchronous)}$ = 1800 rpm
$Speed_{(rated)}$= 1750 rpm $V_{LL(rated)}$ = 230 volts $I_{in(rated)}$ = 19.6 A

LOAD TEST (at rated current)

I_{in} (A)	V_{LL}(V)	P_{in} (KW)	T_o (N-m)	Speed (rpm)	V_{phase}(V)
19.35	205.7	6.1	28.45	1739	118.8

STANDSTILL IMPEDANCE TEST (at rated current)

I_{in} (A)	V_{LL}(V)	P_{in} (KW)	V_{phase}(V)
19.12	48	0.84	27.71

DC TEST (for stator resistance)

	V (volts)	I (A)	R_1 = V/ 2I
A-B	1.63	3	0.272
B-C	1.64	3	0.273
C-A	1.7	3.14	0.271

Calculations

$$X_1 + X_m = (3.V_{LL}^2.I_1^2 - P_{in}^2)^{1/2} / 3.I_1^2$$

$$X_1 + X_m = 2.9\,\Omega$$

$$Z_{in} = V_1 / I_1 = 2.51\,\Omega$$

$$R_1 + R_2 = P_{in} / 3.I_{in}^2 = 0.766\,\Omega$$

$$R_1 = 0.272\,\Omega$$

$$R_2 = 0.494\,\Omega$$

$$X_1 = X_2 = 0.5\,[\,(Z_{in})^2 - (R_1 + R_2)^2\,]^{1/2} = 0.6\,\Omega$$

$$X_m = 2.3\,\Omega$$

E Harmonic analysis for inverters

SQUARE WAVE VSI

Simulated data

V_{L1} = 291.73 V, 97.2% V_{L5}= 57.58 V, 19% V_{L7}= 42.774 V, 14%

THD = 24.6 %

Experimental data

V_{L1} = 206 V, 96% V_{L5}= 42 V, 19.2% V_{L7}= 29 V, 13.7%

THD = 24.6 %

2-LEVEL PWM VSI

Simulated data

V_{L1} = 86.79 V, 98.88% V_{L5}=9.29V, 9.44% V_{L7}= 4.02 V, 4.5%

THD =17.79%

3-LEVEL PWM VSI

Simulated data

V_{L1} = 132.89 V, 91% V_{L5}= 2.59 V, 1.7% V_{L7}= 10.863 V, 14%

THD = 45.86 %

2-LEVEL PWM CSI

Load : L=1.6mH, R=0.272 Ω

SPICE simulation data

Fourier analysis for CSI line current, i(v6):

No. Harmonics: 10, THD: 8.7978%

Magnitude

I_1 = 55.257 A

I_5 = 2.6118 A

I_7 = 3.1228 A

Fourier analysis for motor line current, i(11):

No. Harmonics: 10, THD: 2.2729 %

Magnitude

I_1 = 54.055A

I_5 = 0.1104 A

I_7 = 0.0761 A

F Harmonic analysis data for resonant-mode network rectifier topology

P=7kW, V_{LL} = 202 V, L_s = 7.5mH, C= 34 μF
6-pulse diode bridge (upper bridge line current)
SPICE simulation data
Fourier analysis for i(l6):
No. Harmonics: 10, THD: 6.10703 %, FPF: 1.0, PF: 1.0

	Magnitude	Phase
I_1 =	34.6 A	2.3
I_5 =	1.98 A	-37
I_7 =	0.712 A	-88.096

Experimental data
P=4.4 kW, S= 5.7 kVA
Vab= 198 V, THD=8.44 %, PF=1.0, FPF=1.0
Ia = 16.7 A
I_1 = 13.3 A
I_5 = 9.1 A
I_7 = 6.9 A
I_{11} = 2.9 A
I_{13} = 1.1 A

6-pulse diode bridge (lower bridge line current)
SPICE simulation data
Fourier analysis for i(l9):
No. Harmonics: 10, THD: 8.59562 %, FPF: 0.99, PF: 1.0

	Magnitude	Phase
I_1 =	27.46 A	7.61
I_5 =	2.15979A	-162.11
I_7 =	0.953363A	98.77

Experimental data
P=4.4 kW, S= 5.7 kVA
Vab= 198 V, THD=9.1 %, PF=1.0, FPF=1.0
Ia = 15.8 A
I_1 = 12.6 A
I_3 = 0.9 A
I_5 = 8.1 A
I_7 = 6.3 A
I_{11} = 3.1 A
I_{13} = 1.7 A

12-pulse diode bridge (total input line current))
SPICE simulation data

Fourier analysis for i(16)+i(19):

No. Harmonics: 10, THD: 3.326 %, FPF: 0.964, PF: 0.97

	Magnitude	Phase
I_1 =	58.3828A	-15.22
I_5 =	1.92434A	-104.15
I_7 =	0.25989	117.933

Experimental data

THD=3.42 %, PF=1.0, FPF=1.0

Ia = 32.1 A

I_1 = 12.3 A

I_{11} = 5.1 A

I_{13} = 2.2 A

G SPICE3 Netlist files

G.1 *6-pulse diode bridge rectifier*

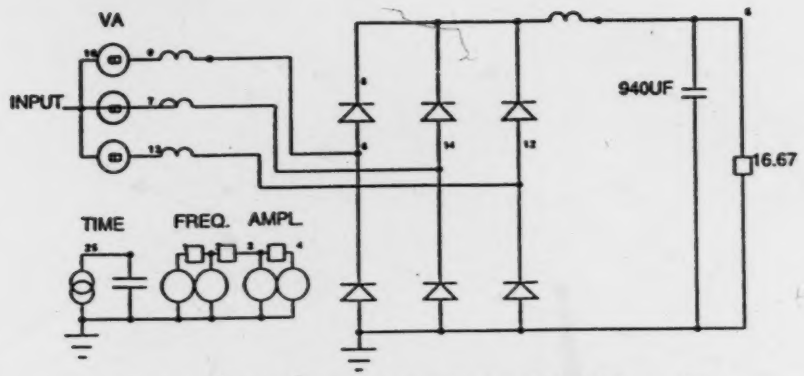

Fig. G.1 SPICE3 schematic for 6-pulse diode bridge rectifier

```
*SPICE_NET
.TRAN 20US 117MS 100MS 20US UIC
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-3
.MODEL PD D
.FOUR 60HZ I(B13)
C1 25 0 1 IC=0
V1 1 0 DC 169
V2 2 0 DC 377
R1 1 2 1K
R2 2 3 1K
V3 3 0 DC 60
V4 4 0 DC 120
R3 3 4 1K
D1 6 8 PD
D2 11 8 PD
.END
D3 0 6 PD
D4 0 11 PD
D5 12 8 PD
D6 0 12 PD
R10 5 0 16.67
B13 9 10 V=V(1)*SIN(V(25)*V(2))
B14 7 10 V=V(1)*SIN(V(25)*V(2)-V(4)/57.296)
B15 13 10 V=V(1)*SIN(V(25)*V(2)-
2*V(4)/57.296)
C8 5 0 940UF
L12 13 12 0.4MH
L13 9 6 0.4MH
L14 7 11 0.4MH
L15 8 5 2.5MH IC=0.0
I1 0 25 1
```

G.2 *12-pulse diode bridge rectifier*

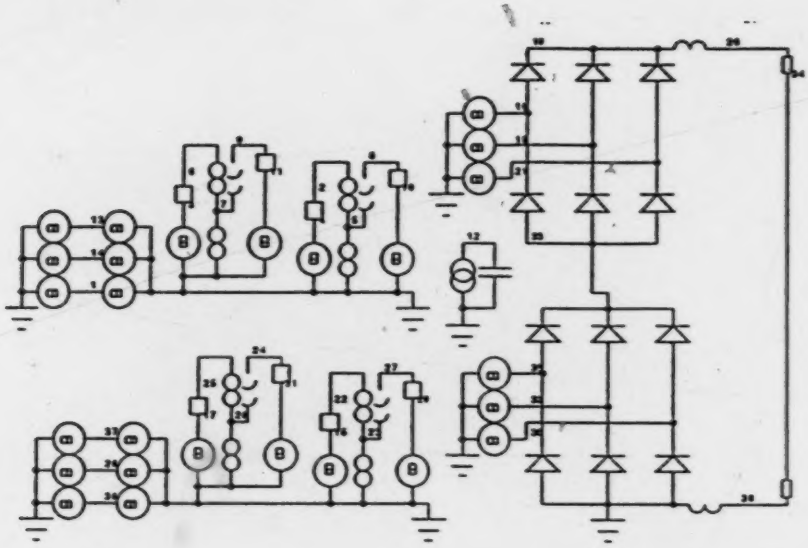

Fig. G.2 SPICE3 schematic for 12-pulse diode bridge rectifier

```
*SPICE_NET
.TRAN 100US 116.67MS 100MS 100US UIC
.MODEL PD D
.OPTIONS METHOD=GEAR ABSTOL=1E-4
RELTOL=0.03
B2 0 1 V=112*SIN(377*V(12)+120/57.296)
B3 1 0 I=-0.5*(I(B5)+1.732*I(B6))
B4 14 0 I=0.5*(-I(B5)+1.732*I(B6))
B5 4 0 V=(2*V(13)-V(14)-V(1))/3
B6 3 0 V=(V(14)-V(1))*0.57735
R1 2 4 .3
L1 2 5 .97MH
R2 3 6 .3
L2 6 7 .97MH
L3 5 8 .608MH
L4 7 9 .608MH
L5 5 0 .97H
L6 7 0 .97
R3 8 10 .188
R4 9 11 .188
I1 0 12 1
C1 12 0 1 IC=0
B7 0 13 V=112*SIN(377*V(12))
B8 13 0 I=I(B5)
B12 10 0 V=(2*V(16)-V(18)-V(21))/3
B13 0 16 I=I(B12)
B14 0 21 I=-0.5*(I(B12)+1.732*I(B16))
B15 0 18 I=0.5*(-I(B12)+1.732*I(B16))
B16 11 0 V=(V(18)-V(21))*0.57735
D4 16 19 PD
D5 18 19 PD
D6 21 19 PD
D7 33 16 PD
D8 33 18 PD
D9 33 21 PD
B17 15 0 V=(2*V(37) -V(28) -V(36))/3
B18 17 0 V=(V(28) - V(36))*0.57735
R12 22 15 .3
L7 22 23 .97MH
R13 17 25 .3
L8 25 26 .97MH
L9 23 27 .608MH
L10 26 24 .608MH
L11 23 0 .97H
```

```
L12 26 0 .97
R14 27 29 .188
R15 24 31 .188
B19 29 0 V=(V(35)-V(32))*0.57735
B20 31 0 V=-(2*V(30) - V(35) -V(32))/3
B21 0 35 I=I(B19)
B22 0 30 I=-0.5*(I(B19) + 1.732*I(B20))
B23 0 32 I=0.5*(-I(B19) + 1.732*I(B20))
D11 35 33 PD
D12 32 33 PD
D13 30 33 PD
D14 0 35 PD
D15 0 32 PD
D16 0 30 PD
B30 0 28 V=112*SIN(377*V(12)-120/57.296)
B31 0 36 V=112*SIN(377*V(12)+120/57.296)
B32 36 0 I=-0.5*(I(B17)+1.732*I(B18))
B33 28 0 I=0.5*(-I(B17)+1.732*I(B18))
B34 0 37 V=112*SIN(377*V(12))
B35 37 0 I=I(B17)
L13 19 20 2.5MH
L14 38 0 2.5MH
R16 20 34 20.833
R18 34 38 20.8333
B1 0 14 V=112*SIN(377*V(12)-120/57.296)
.END
```

G.3 *Square wave Voltage Source Inverter*

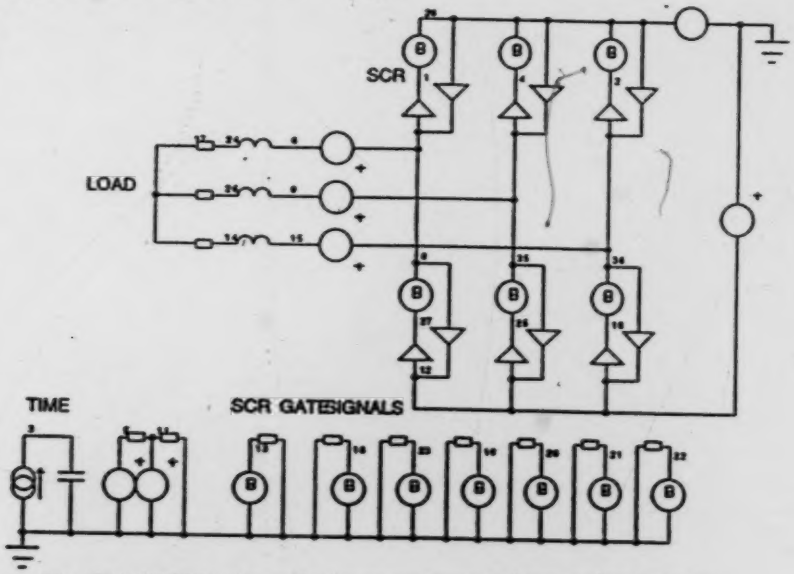

Fig. G.3 SPICE3 schematic for square wave voltage source inverter

```
*SPICE_NET
.TRAN 25US 140MS 100MS 25US UIC
.MODEL PD D
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-4
B2 28 4 V=I(B2)*(V(22)*0.05 + (1-V(22))*1E4)
B3 28 2 V=I(B3)*(V(20)*0.05 + (1-V(20))*1E4)
B4 8 27 V=I(B4)*(V(21)*0.05 + (1-V(21))*1E4)
B5 35 25 V=I(B5)*(V(19)*0.05 + (1-V(19))*1E4)
B6 36 18 V=I(B6)*(V(16)*0.05 + (1-V(16))*1E4)
D1 8 1 PD
D2 35 4 PD
D3 36 2 PD
D4 12 27 PD
D5 12 25 PD
D6 12 18 PD
V1 28 0 DC 0
V2 0 12 DC -275
```

```
V3 8 6 DC 0
L1 24 6 6MH IC=0
R1 24 17 4.94
V4 35 9 DC 0
V5 36 15 DC 0
L2 26 9 6MH IC=0
L3 14 15 6MH IC=0
R2 26 17 4.94
R3 14 17 4.94
I1 0 3 1
C1 3 0 1 IC=0
V6 5 0 DC 377
V7 11 0 DC 60
R4 11 5 1K
R5 0 11 1K
B7 13 0 V=ASIN(SIN(V(3)*V(5)))
R6 0 13 1K
B8 16 0 V=U(V(13))
R7 16 0 1K
B9 23 0 V=U(ASIN(SIN(V(3)*V(5) -
V(11)/57.296)))
B10 19 0 V=U(ASIN(SIN(V(3)*V(5) -
2*V(11)/57.296)))
B11 20 0 V=U(ASIN(SIN(V(3)*V(5) -
3*V(11)/57.296)))
B12 21 0 V=U(ASIN(SIN(V(3)*V(5) -
4*V(11)/57.296)))
R8 23 0 1K
R9 19 0 1K
R10 20 0 1K
R11 21 0 1K
B13 22 0 V=U(ASIN(SIN(V(3)*V(5) -
5*V(11)/57.296)))
R12 22 0 1K
D7 28 8 PD
D8 28 35 PD
D9 28 36 PD
D10 8 12 PD
D11 35 12 PD
D12 36 12 PD
B1 28 1 V=I(B1)*(V(23)*0.05 + (1-V(23))*1E4)
.END
```

G.4 *PWM Voltage Source Inverter*

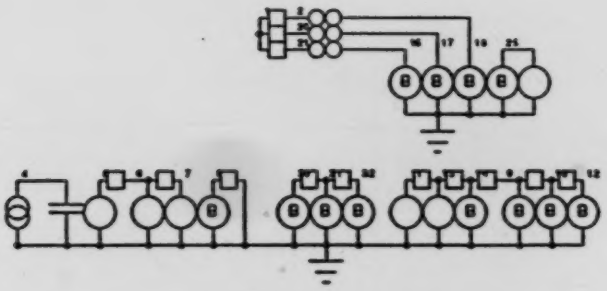

Fig. G.4 SPICE3 schematic for PWM VSI

```
*SPICE_NET
.TRAN 20US 116.67MS 100MS 20US UIC
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-3
C1 4 0 1 IC=0
V1 5 0 DC 377
R1 5 6 1K
V2 6 0 DC 100
V3 7 0 DC 120
R2 6 7 1K
B1 8 0 V=ASIN(SIN(V(4)*V(5)))
B2 30 0 V=SIN(V(5)*V(4))
B3 31 0 V=SIN(V(5)*V(4)-V(7)/57.296)
```

```
B4 32 0 V=SIN(V(5)*V(4)+V(7)/57.296)
R3 8 0 1K
R4 30 31 1K
R5 31 32 1K
B5 15 0 V=V(25)*V(9)
B6 17 0 V=V(25)*V(10)
B7 18 0 V=V(25)*V(12)
L1 18 2 1.6MH
L2 17 20 1.6MH
L3 15 21 1.6MH
R6 1 2 .494
R7 1 20 .494
R8 1 21 .494
B8 25 0 I=-I(B5)*V(9)-I(B6)*V(10)-I(B7)*V(12)
V4 25 0 DC 275
V5 11 0 DC 7539.822
R9 11 13 1K
V6 13 0 DC 1.05
R10 13 14 1K
B10 14 0 V=V(13)*ASIN(SIN(V(11)*V(4)))
R11 14 9 1K
B11 9 0 V=U(V(30,14))
R12 9 10 1K
B12 10 0 V=U(V(31,14))
R13 10 12 1K
B13 12 0 V=U(V(32,14))
I1 0 4 1
.END
```

G.5 *PWM Current Source Inverter*

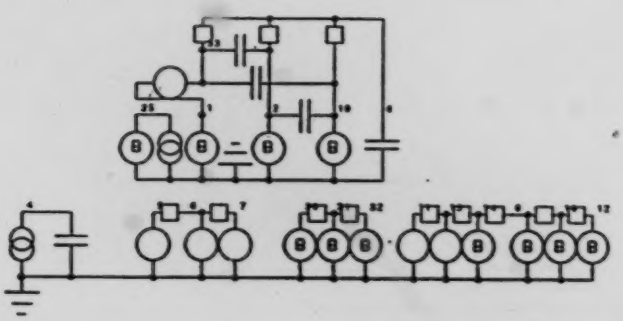

Fig. G.5 SPICE3 schematic for PWM CSI

```
*SPICE_NET
.TRAN 100US 116.67MS 100MS 100US UIC
.MODEL PD D
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-4
C1 4 0 1 IC=0
V1 5 0 DC 377
R1 5 6 1K
V2 6 0 DC 100
V3 7 0 DC 120
R2 6 7 1K
B5 1 0 I=I(B8)*V(9,10)
B6 2 0 I=I(B8)*V(10,12)
B7 19 0 I=-I(B8)*(V(9,10)+V(10,12))
B8 25 0 V=V(33)*V(9)+V(2)*V(10)+V(19)*V(12)
I2 25 0 100
C2 19 2 100UF IC=0
C3 2 33 100UF IC=0
C4 19 33 100UF IC=0
B9 30 0 V=SIN(V(5)*V(4))
B10 31 0 V=SIN(V(5)*V(4)-V(7)/57.296)
```

```
B11 32 0 V=SIN(V(5)*V(4)+V(7)/57.296)
R9 30 31 1K
R10 31 32 1K
V4 11 0 DC 7539.822
R11 11 13 1K
V5 13 0 DC 1.05
R12 13 14 1K
B12 14 0 V=V(13)*ASIN(SIN(V(11)*V(4)))
R13 14 9 1K
B13 9 0 V=U(V(30,14))
R14 9 10 1K
B14 10 0 V=U(V(31,14))
R15 10 12 1K
B15 12 0 V=U(V(32,14))
V7 33 1 DC 0
C6 8 0 1NF IC=0
R16 8 33 10
R17 8 2 10
R18 8 19 10
I1 0 4 1
.END
```

G.6 *Induction Motor*

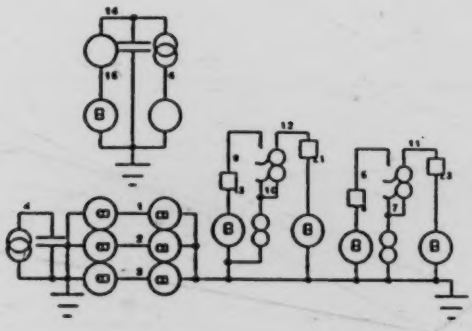

Fig. G.6 SPICE3 schematic for induction motor

```
*SPICE_NET
.TRAN 100US 800MS 0 100US UIC
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-4
.PRINT TRAN I(V2) V(16) I(B9)
B2 3 0 V=155.6*SIN((V(4)+120)/57.296)
B3 3 0 I=0.5*(I(B5)-1.732*I(B6))
B4 2 0 I=0.5*(I(B5)+1.732*I(B6))
B5 8 0 V=(2*V(1)-V(3)-V(2))/3
B6 13 0 V=(V(2)-V(3))*0.57735
R1 5 8 .295
L1 7 5 .944MH IC=0
R2 13 9 .295
L2 10 9 .944MH IC=0
L3 11 7 .944MH IC=0
L4 12 10 .944MH IC=0
L5 7 0 35.15MH IC=0
L6 10 0 35.15MH IC=0
R3 11 23 .201
R4 12 21 .201
I1 0 4 DC 21600
C1 4 0 1 IC=0
B7 1 0 V=155.6*SIN(V(4)/57.296)
B8 1 0 I=-I(B5)
B9 23 0 V=-0.03516*V(16)*(-I(B6)-1.027*I(B10))
B10 21 0 V=0.03516*V(16)*(-I(B5)-1.027*I(B9))
B11 15 0 I=-0.03516*(I(B6)*I(B9)-I(B5)*I(B10))
V1 15 16 DC 0
C2 16 0 26MF IC=0
```

```
V2 6 0 DC 0
I2 16 6 5
B1 2 0 V=155.6*SIN((V(4)-120)/57.296)
.END
```

G.7 *12-pulse, 3-level PWM VSI drive*

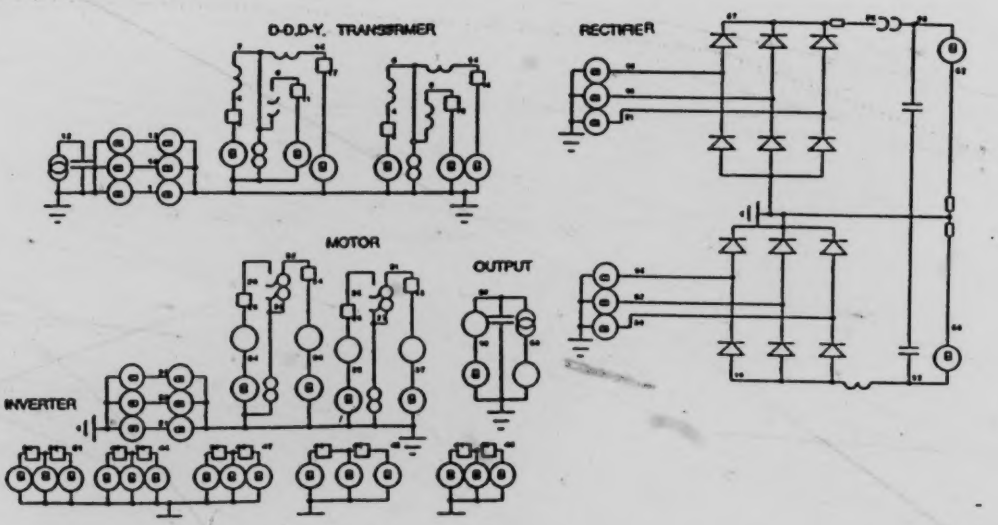

Fig. G.7 SPICE3 schematic for 12-pulse, 3-level Inverter Drive

```
C:\SPICE\mot/3ldy
*SPICE_NET
.TRAN 25uS 150MS 100MS 25uS UIC
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-4
.MODEL PD D
B2 0 1 V=69*SIN(377*V(12)+120/57.296)
B3 1 0 I=-0.5*(I(B5)+1.732*I(B6))
B4 14 0 I=0.5*(-I(B5)+1.732*I(B6))
B5 4 0 V=(2*V(13)-V(14)-V(1))/3
B6 3 0 V=(V(14)-V(1))*0.57735
R1 6 4 .3
L1 6 5 .97MH
R2 3 8 .3
L2 8 7 .97MH
L3 5 10 .608MH
L4 7 2 .608MH
L5 5 0 .97H
L6 7 0 .97
R3 10 9 .188
R4 2 11 .188
I1 0 12 1
C1 12 0 1 IC=0
```

```
B7 0 13 V=69*SIN(377*V(12))
B8 13 0 I=I(B5)
B9 9 0 V=(2*V(16)-V(18)-V(21))/3
B10 11 0 V=(V(18)-V(21))*0.57735
L9 5 24 .608MH
L10 7 22 .608MH
R7 24 29 .188
R8 22 31 .188
B13 29 0 V=(V(35)-V(32))*0.57735
B14 31 0 V=-(2*V(30) - V(35) -V(32))/3
B21 100 16 I=I(B9)
v100 100 0 dc 0
B22 0 21 I=-0.5*(I(B9)+1.732*I(B10))
B23 0 18 I=0.5*(-I(B9)+1.732*I(B10))
D1 16 57 PD
D2 18 57 PD
D3 21 57 PD
D4 74 16 PD
D5 74 18 PD
D6 74 21 PD
B24 0 35 I=I(B13)
B25 0 30 I=-0.5*(I(B13) + 1.732*I(B14))
B26 0 32 I=0.5*(-I(B13) + 1.732*I(B14))
D7 35 74 PD
D8 32 74 PD
D9 30 74 PD
D10 0 35 PD
D11 0 32 PD
D12 0 30 PD
B27 15 0 I=-0.03516*(I(V3)*I(V6)-I(V4)*I(V5))
V2 15 39 DC 0
C2 39 0 26MF IC=0
B28 59 0 I=0.5*(-I(V5)+1.732*I(V3))
B29 51 0 I=0.5*(-I(V5)-1.732*I(V3))
B30 40 0 V=(2*V(50)-V(51)-V(59))/3
B31 49 0 V=(V(51)-V(59))*0.57735
R10 53 41 .295
L13 55 53 .944MH IC=0
R11 47 48 .295
L14 45 48 .944MH IC=0
L15 90 55 .944MH IC=0
L16 44 45 .944MH IC=0
L17 55 0 35.15MH IC=0
L18 45 0 35.15MH IC=0
R12 90 38 .201
R13 44 43 .201
B32 50 0 I=I(V5)
B33 42 0 V=0.03516*V(39)*(I(V5)+1.027*I(V6))
V3 49 47 DC 0
V4 42 43 DC 0
V5 40 41 DC 0
V6 34 38 DC 0
B34 50 0 V=V(69)*V(65)*V(23,74)-(V(69)-
1)*V(65)*V(74,33)
B35 51 0 V=V(62)*V(72)*V(23,74)-(V(62)-
1)*V(72)*V(74,33)
B36 59 0 V=V(68)*V(73)*V(23,74)-(V(68)-
1)*V(73)*V(74,33)
B46 34 0 V=-0.03516*V(39)*(I(V3)+1.027*I(V4))
L19 75 23 2.5MH
D13 46 76 PD
D14 56 76 PD
D15 0 46 PD
D16 0 56 PD
R30 76 0 20
V14 60 0 DC 10
R31 60 61 1K
B48 56 46 V=V(60)*ASIN(SIN(V(12)*V(19)*10))
D17 77 89 PD
D18 78 89 PD
D19 0 77 PD
D20 0 78 PD
R32 89 0 20
B49 78 77 V=V(60)*ASIN(SIN(V(12)*V(19)*10-
120/57.296))
D21 82 83 PD
D22 84 83 PD
D23 0 82 PD
D24 0 84 PD
R34 83 0 20
B50 84 82
V=V(60)*ASIN(SIN(V(12)*V(19)*10+120/57.296
))
B51 62 0 V=U(SIN(V(12)*V(61)-120/57.296))
B52 63 0 V=V(69)*V(76)+(V(69)-1)*V(76)
B53 64 0 V=12*SIN(V(12)*V(61))
B54 65 0 V=V(69)*U(V(64,63)) + (V(69)-
1)*U(V(63,64))
B55 66 0 V=12*SIN(V(12)*V(61)-120/57.296)
B56 67 0 V=12*SIN(V(12)*V(61)+120/57.296)
R35 64 66 1K
R36 66 67 1K
```

```
R37 62 68 1K
B57 68 0 V=U(SIN(V(12)*V(61)+120/57.296))
R39 69 62 1K
B58 69 0 V=U(SIN(V(12)*V(61)))
R40 63 70 1K
B59 70 0 V=V(62)*V(89)+(V(62)-1)*V(89)
R41 70 71 1K
B60 71 0 V=V(68)*V(83)+(V(68)-1)*V(83)
R42 65 72 1K
B61 72 0 V=V(62)*U(V(66,70)) + (V(62)-
1)*U(V(70,66))
R43 72 73 1K
B62 73 0 V=V(68)*U(V(67,71)) + (V(68)-
1)*U(V(71,67))
C5 23 74 10UF IC=0.0
C6 74 33 10UF IC=0.0
B63 23 52 I=-I(B36)-I(B35)-I(B34)
B64 58 33 I=-I(B36)-I(B35)-I(B34)
R44 74 58 .01
R45 52 74 .01
L21 33 0 2.5MH
R46 57 75 0.01
V17 0 17 DC 0
I3 39 17 5
V19 61 0 DC 377
R48 19 61 1K
B66 19 0 V=U(V(12)-200)*377 + U(200-
V(12))*345.4
B1 0 14 V=69*SIN(377*V(12)-120/57.296)
.END
```

G.8 *Novel Rectifier Topology*

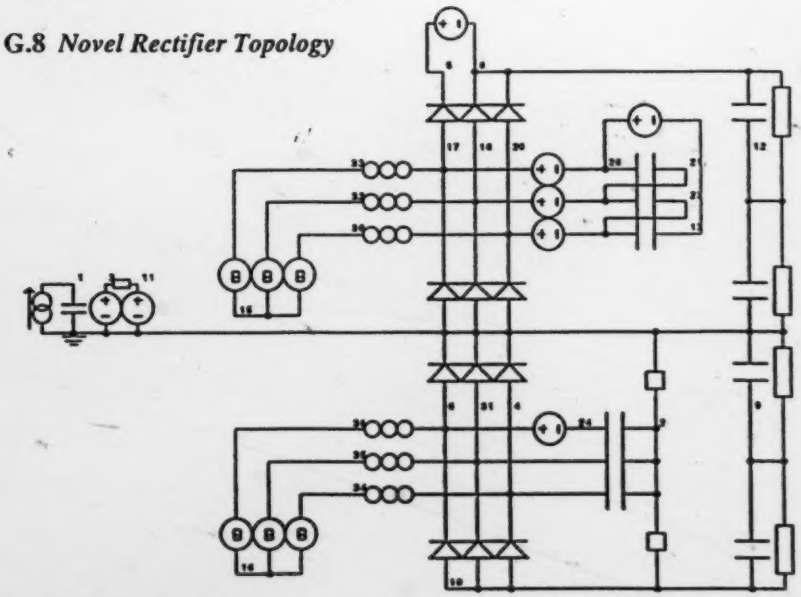

Fig. G.8 SPICE3 schematic for 12-pulse rectifier with resonant mode harmonic correction circuit.

```
*SPICE_NET
.TRAN 2US 117MS 100MS 2US UIC
.OPTIONS METHOD=GEAR RELTOL=0.03
ABSTOL=1E-4
.MODEL PD D(IS=1E-20 BV=1200 CJO=1PF
TT=0)
.FOUR 60HZ I(L6) I(L9) I(L6)+I(L9)
I2 1 0 DC -1
```

```
V3 3 0 DC 202
R3 3 11 1
V4 11 0 DC 60
C10 28 21 40UF IC=0
D15 20 8 PD
D16 0 17 PD
D17 0 18 PD
D18 0 20 PD
C15 8 12 1MF IC=150
C16 12 0 1MF IC=150
R11 8 12 5
R12 12 0 5
L6 33 17 7.5MH IC=0
L7 32 18 7.5MH IC=-20
L8 30 20 7.5MH IC=20
D24 10 4 PD
C20 0 9 1MF IC=150
C21 9 10 1MF IC=150
R13 0 9 5
R14 9 10 5
L9 36 6 7.5MH IC=-14
B22 34 16
V=0.816*V(3)*SIN(6.283*V(1)*V(11)+1.571)
C22 24 2 40UF IC=-100
C23 31 2 40UF IC=-100
C24 4 2 40UF IC=200
V6 17 28 DC 0
V7 18 21 DC 0
V8 20 23 DC 0
V9 5 8 DC 0
V10 6 24 DC 0
R44 0 2 10K
R45 2 10 10K
V11 28 13 DC 0
R45 2 10 10K
V11 28 13 DC 0
C7 1 0 1 IC=0
C12 21 23 40UF IC=-280
C14 23 13 40UF IC=280
D13 17 5 PD
D14 18 8 PD
B15 33 15 V=0.816*V(3)*SIN(6.283*V(1)*V(11))
B18 32 15 V=0.816*V(3)*SIN(6.283*V(1)*V(11)-
2.0944)
B19 30 15
V=0.816*V(3)*SIN(6.283*V(1)*V(11)+2.0944)
D19 6 0 PD
D20 31 0 PD
D21 4 0 PD
D22 10 6 PD
D23 10 31 PD


L10 35 31 7.5MH IC=-14
L11 34 4 7.5MH IC=28
B20 36 16 V=0.816*V(3)*SIN(6.283*V(1)*V(11)-
0.5236)
B21 35 16 V=0.816*V(3)*SIN(6.283*V(1)*V(11)-
2.618)

V7 18 21 DC 0
V8 20 23 DC 0
V9 5 8 DC 0
V10 6 24 DC 0
R44 0 2 10K



.END
```

G.9 *Run file for constant V/F curves for induction machine*

SPICE3 run file

```
*torque speed curves for an induction motor
* a = the per-unit speed setting
* Fs = the base frequency seting of 60Hz
* P = # of poles
* Vll = base line-line voltage at 60Hz = 208V
* Vlla = motor line-line voltage at the per-unit speed setting a
* F1 = motor supply frequency at the per-unit speed setting a
* Ns = motor synchronous speed at the per-unit speed setting a
* Ws = motor synchronous speed at the per-unit speed setting a
* Nr = rotor speed at the speed setting a and slip
* Wr = rotor speed at the speed setting a and slip
* slip = motor slip
* Rs,Ls,Rr,Lr,Lm are the motor equivalent circuit parameters
* K1,K2 are constants required in the dq-axis equivalent circuit
* Imo is the initialization current for Im in the d-axis equivalent circuit.
.controlc
set width=275; set nobreak; set noheader; set noprintscale
source im
let Fs=60;let P=2;let a=0.4;let Vll=208;let torque=0;let Vlla=a*Vll;let F1=a*Fs
let Ns=a*Fs*120/P;let Ws=Ns*3.1425927/30;let Nr=Ns;let Wr=Ws
let Rs=0.295;let Rr=0.201;let Ls=0.000944;let Lr=0.000944;let Lm=0.03515;let
K1=3*P*Lm/2;let K2=1+Lr/Lm
let Vlla=a*Vll;let F1=a*Fs;let Imo=0.816*Vll/(6.283*Fs*(Ls+Lm))

let slip=0.0
while slip lt 1
let Nr=(1-slip)*Ns;let Wr=Nr*3.1415927/30
alter v4=F1;alter v5=Vlla;alter v3=Wr;alter v7=K1;alter v6=K2
alter r1=Rs;alter r2=Rs;alter r3=Rr;alter r4=Rr
alter l1=Ls;alter l2=Ls;alter l3=Lr;alter l4=Lr;alter l5=Lm;alter l6=Lm
alter l1 ic=Imo; alter l5 ic=-Imo
tran 125uS 875mS 750mS 125uS uic
let torque=mean(i(V3));let time=v(4)
let va=v(1);let vb=v(2);let vc=v(3);let ia=-i(b7);let ib=-i(b1);let ic=-i(b2)
let vab=va-vb; let vbc=vb-vc;let vca=vc-va
let iabc=sqrt((mean(ia^2)+mean(ib^2)+mean(ic^2))/3);
let vabc=sqrt((mean(vab^2)+mean(vbc^2)+mean(vca^2))/3);
let pabc=mean(vab*ia)-mean(vbc*ic);let apabc=sqrt(3)*iabc*vabc;let
pfabc=pabc/apabc
let pout=torque*Wr; let eff=100*pout/pabc

print col Nr slip torque pout iabc pabc pfabc eff
```

```
destroy all
let slip=slip+0.01
end
.endc
end
```

Mathematica run file

```
L1=0.944;L2=0.944;Lm=35.15;R1=0.295;R2=0.201;VL=208;P=4;

Zf[a_,slip_]:=1/(1/(R2/slip+I*0.377*a*L2)+1/(I*0.377*a*Lm));
Zph[a_,slip_]:=(R1 + I*0.377*a*L1)+Zf[a,slip];V1[a_]:=a*VL/Sqrt[3];
Iph[a_,slip_]:=N[V1[a]/Zph[a,slip]];Imag[a_,slip_]:=Abs[Iph[a,slip]];
Pe[a_,slip_]:=N[3*(Imag[a,slip]^2)*Re[Zf[a,slip]]];
Pin[a_,slip_]:=N[3*(Imag[a,slip]^2)*Re[Zph[a,slip]]]/1000;
VA[a_,slip_]:=Sqrt[3]*Imag[a,slip]*a*VL/1000;
PF[a_,slip_]:=Pin[a,slip]/VA[a,slip];
Ns[a_]:=(2/P)*a*3600;Nr[a_,slip_]:=N[(1-slip)*Ns[a]];
Te[a_,slip_]:=N[Pe[a,slip]/(Ns[a]/9.549)];
Pout[a_,slip_]:=Te[a,slip]*Nr[a,slip]/(1000*9.549);
Eff[a_,slip_]:=100*Pout[a,slip]/Pin[a,slip];

steps=200;
dat10=Table[i,{i,1,steps},{j,1,6}];dat08=Table[i,{i,1,steps},{j,1,6}];dat06=Table[i,{i,1,steps},{j,
dat04=Table[i,{i,1,steps},{j,1,6}];dat02=Table[i,{i,1,steps},{j,1,6}];
slip=0;Do[slip=slip+1/steps;
dat10[[i,1]]=Nr[1,slip];dat10[[i,2]]=Imag[1,slip];dat10[[i,3]]=Te[1,slip];
dat10[[i,4]]=PF[1,slip];dat10[[i,5]]=Pin[1,slip];dat10[[i,6]]=Eff[1,slip];
dat08[[i,1]]=Nr[0.8,slip];dat08[[i,2]]=Imag[0.8,slip];dat08[[i,3]]=Te[0.8,slip];
dat08[[i,4]]=PF[0.8,slip];dat08[[i,5]]=Pin[0.8,slip];dat08[[i,6]]=Eff[0.8,slip];
dat06[[i,1]]=Nr[0.6,slip];dat06[[i,2]]=Imag[0.6,slip];dat06[[i,3]]=Te[0.6,slip];
dat06[[i,4]]=PF[0.6,slip];dat06[[i,5]]=Pin[0.6,slip];dat06[[i,6]]=Eff[0.6,slip];
dat04[[i,1]]=Nr[0.4,slip];dat04[[i,2]]=Imag[0.4,slip];dat04[[i,3]]=Te[0.4,slip];
dat04[[i,4]]=PF[0.4,slip];dat04[[i,5]]=Pin[0.4,slip];dat04[[i,6]]=Eff[0.4,slip];
dat02[[i,1]]=Nr[0.2,slip];dat02[[i,2]]=Imag[0.2,slip];dat02[[i,3]]=Te[0.2,slip];
dat02[[i,4]]=PF[0.2,slip];dat02[[i,5]]=Pin[0.2,slip];dat02[[i,6]]=Eff[0.2,slip],{i,steps}];
```

G.10 *Run file for Novel Rectifier Topology performance curves*

```
scr resonant circuit
.controlc

source c
let nz=1.0; let nfstart=2; let nfstep=0.2; let nfstop=10
let Fbase=60;let Vll=202;let Pbase=7000
let Vph=Vll/sqrt(3);let Vm=Vph/sqrt(2);let Wbase=Fbase*6.28319
let Ibase=Pbase/(Vll*sqrt(3)); let Zbase=Vph/Ibase;
```

```
let nf=nfstart;let zo=nz*Zbase; let fo=nf*Fbase;let wo=6.28319*fo
let lo=zo/wo;let co=1/(wo*zo);let cll=co/3;let cph=co/2
print col nz nfstart nfstep nfstop>f1.0.abc
print col nz nfstart nfstep nfstop>f1.0.xyz
print col nz nfstart nfstep nfstop>f1.0.12pulse
set width=275; set nobreak; set noheader; set noprintscale
let cr=15E-6; let lac=10E-3; let rld=6
let pabc=0; let thdabc=0; let pfabc=0; let phabc=0; let mnabc=0; let pabc=0
let pxyz=0; let thdxyz=0; let pfxyz=0; let phxyz=0; let mnxyz=0; let pxyz=0
let paa=0; let thd=0; let pfaa=0; let ph=0; let mn=0; let paa=0
let mnabc=0;let mnxyz=0; let mn=0

let nf=nfstart
while nf lt nfstop
let count=0
let zo=nz*Zbase; let fo=nf*Fbase;let wo=6.28319*fo
let lo=zo/wo;let co=1/(wo*zo);let cll=co/3;let cph=co/2

while count lt 4
alter v4=Fbase;alter v3=Vll
alter l6=lo; alter l7=lo; alter l8=lo;alter l9=lo; alter l10=lo; alter l11=lo
alter c10=cll; alter c12=cll; alter c14=cll;alter c22=co; alter c23=co; alter c24=co
alter r11=rld;alter r12=rld;alter r13=rld;alter r14=rld
tran 2uS 250mS 200mS 2uS uic

let time=v(1)
let va=v(33,15);let vb=v(32,15);let vc=v(30,15);let ia=i(l6);let ib=i(l7);let ic =i(l8)
let vab=va-vb; let vbc=vb-vc;let vca=vc-va
let iabc=sqrt((mean(ia^2)+mean(ib^2)+mean(ic^2))/3);
let vabc=sqrt((mean(vab^2)+mean(vbc^2)+mean(vca^2))/3);
let pabc=mean(vab*ia)-mean(vbc*ic);let apabc=sqrt(3)*iabc*vabc;let
pfabc=pabc/apabc
let i1rabc=sqrt(2)*mean(ia*sin(Wbase*time));
let i1iabc=sqrt(2)*mean(ia*cos(Wbase*time))
let i1abc=sqrt(i1rabc^2+i1iabc^2);let phabc=atan(i1iabc/i1rabc)
let ifabc=(abs(i1rabc)/i1rabc)*sqrt(2)*i1abc*sin(Wbase*time+phabc)
let ihabc=ia-ifabc;let ihrmsabc=sqrt(mean(ihabc^2)); let thdabc=100*ihrmsabc/i1abc

let vx=v(36,16);let vy=v(35,16);let vz=v(34,16);let ix=i(l9);let iy=i(l10);let iz=i(l11)
let vxy=vx-vy; let vyz=vy-vz;let vzx=vz-vx
let ixyz=sqrt((mean(ix^2)+mean(iy^2)+mean(iz^2))/3)
let vxyz=sqrt((mean(vxy^2)+mean(vyz^2)+mean(vzx^2))/3)
let pxyz=mean(vxy*ix)-mean(vyz*iz);let apxyz=sqrt(3)*ixyz*vxyz;let pfxyz=pxyz/ap
xyz
let i1rxyz=sqrt(2)*mean(ix*sin(Wbase*time))
```

```
let i1ixyz=sqrt(2)*mean(ix*cos(Wbase*time))
let i1xyz=sqrt(i1rxyz^2+i1ixyz^2);let phxyz=atan(i1ixyz/i1rxyz)
let ifxyz=(abs(i1rxyz)/i1rxyz)*sqrt(2)*i1xyz*sin(Wbase*time+phxyz)
let ihxyz=ix-ifxyz;let ihrmsxyz=sqrt(mean(ihxyz^2)); let thdxyz=100*ihrmsxyz/i1xyz
let ia1=(ix-iy)/sqrt(3); let ib1=(iy-iz)/sqrt(3); let ic1=(iz-ix)/sqrt(3)
let iaa=ia+ia1;let ibb=ib+ib1;let icc=ic+ic1
let irmsaa=sqrt((mean(iaa^2)+mean(ibb^2)+mean(icc^2))/3)
let paa=mean(vab*iaa)-mean(vbc*icc);let apaa=sqrt(3)*irmsaa*vabc;let
pfaa=paa/apaa
let i1r=sqrt(2)*mean(iaa*sin(Wbase*time));
let i1i=sqrt(2)*mean(iaa*cos(Wbase*time))
let i1=sqrt(i1r^2+i1i^2);let ph=atan(i1i/i1r)
let if=(abs(i1r)/i1r)*sqrt(2)*i1*sin(Wbase*time+ph)
let ih=iaa-if;let ihrms=sqrt(mean(ih^2)); let thd=100*ihrms/i1

let phabc=phabc*57.296;let phxyz=phxyz*57.296+30;let ph=ph*57.296
let rld=rld*pabc/Pbase
let mn=mean(v(5));let mnabc=mn/vll;let mn=-mean(v(7));let mnxyz=mn/vll;
let mn=(mnabc+mnxyz)/2

let count=count+1
destroy all
end

print nz
print col nz nf lo co cph cll rld pabc thdabc pfabc phabc mnabc>>f1.0.abc
print col nz nf lo co cph cll rld pxyz thdxyz pfxyz phxyz mnxyz>>f1.0.xyz
print col nz nf lo co cph cll rld paa thd pfaa ph mn>>f1.0.12pulse
let nf=nfstep+nf;let rld=6
end

.endc
.end
```

SPICE3 simulation techniques in power electronics

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ABSTRACT

This paper describes numerous SPICE3 techniques appropriate for Power Electronics. The recent updates made to SPICE at the University of Berkely has made obsolete various SPICE simulation techniques often used in Power Electronics systems. Many new features have also been added to SPICE3 that allow many new circuit design oriented tasks to be performed. The introduction of the "B-statement", and the comparison statements, the "U-ramp" and "U-statement" has simplified the structure of control and switching functions used frequently for Power Electronics. Various simulation techniques are illustrated with the use of a variable speed drive configuration using a ΔΔ, ΔY input transformer. The current source inverter uses a phase controlled rectifier to regulate the DC link current. The voltage source inverter uses a PWM technique to provide a low THD current on the induction motor side. The paper describes how d-q axis modeling in SPICE3 can be used to model the induction motor and the transformer. Experimental results are used to verify the SPICE3 simulations

1.INTRODUCTION

A variable speed AC machine connected to the rectifier-inverter system gives rise to complex stability problems. The machine is a non-linear multivariable system and interacts dynamically with the source impedance of the drive. Further complexity may arise when for instance multiple machines are fed by a single inverter or multiple rectifiers feed a single inverter. The analysis of such systems is tedious and computer simulation becomes imperative. The study of new control strategies, the effect of harmonics and the variation of system parameters are also facilitated by simulation results. The comparison of simulation results with experimental ones suggest new ways of improving existing drive topologies.

This paper describes various simulation techniques that can be implemented using Spice3 programming language to simulate large complex power electronic drive systems.

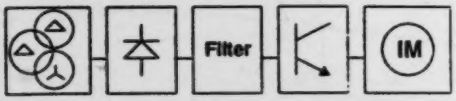


Fig.1 General Drive Structure

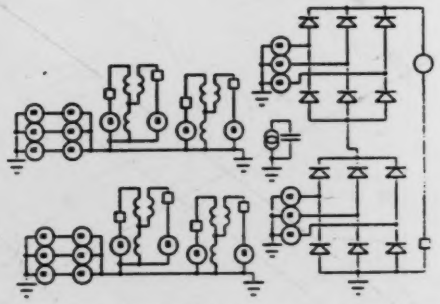


Fig. 2 Spice3 schematic for ΔΔ,ΔY transformer and rectifiers

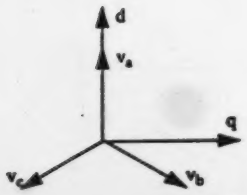
2. TRANSFORMER SIMULATION

The equivalent per phase circuit is considered in terms of d-q axis theory. In this theory the time varying parameters are eliminated and the variables and parameters are expressed in orthogonal or mutually decoupled direct (d) and quadrature (q) axes. The supply voltages are given by the transformation where v_o is the zero sequence component which does not exist for balanced 3-phase conditions.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta & 1 \\ \sin(\theta-120°) & \cos(\theta-120°) & 1 \\ \sin(\theta+120°) & \cos(\theta+120°) & 1 \end{bmatrix} \cdot \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix}$$

Setting θ=0, the d-axis will coincide with v_a and ignoring the zero sequence component, the above matrix equation yields the following transformation relations:

$$v_d = (2v_a - v_b - v_c)/3$$
$$v_q = (v_b - v_c)/3$$



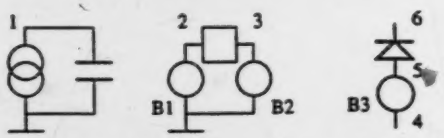
The ΔΔ transformer is modeled by considering two separate d-q per phase equivalent circuits having identical parameters. Each phase is fed with v_d and v_q respectively by means of the B-statement. The supply side currents are a function of the currents flowing in the respective primaries. Similarly the load side currents are function of the secondary currents.

The Δ-Y model differs from the ΔΔ model in that its output voltages are 30° phase shifted from that of the ΔΔ. A SPICE3 simulated schematic for the ΔΔ and ΔY transformers is given in fig.2.

3. RECTIFIERS

The series connections of two diode bridges, fed from a ΔΔ ΔY transformer, gives a 12 pulse rectification. This constant DC output is fed to the input stage of a Voltage Source Inverter (VSI). In contrast, the Current Source Inverter (CSI) requires phase control rectification. The output of the simulated series connected rectifiers yields results similar to the experimental plots, as shown in fig.4 and fig.5.

The switching device in an scr bridge is modeled by having a diode in series with a B-statement. The diode maintains the unidirectional property of the device.(see Fig.3).



(a) node for time (b) switching pattern (c) scr switch

```
B1 2  0 v = asin(sin(377*v(1)-90/57.296))
B2 3  0 v = u(v(2))
B3 5  4 v = i(B3)*(v(3)*0.05+(1-v(3))/1E6)
D1 6  5 PD
```

(d) spice3 text listing

Fig. 3 Spice3 models

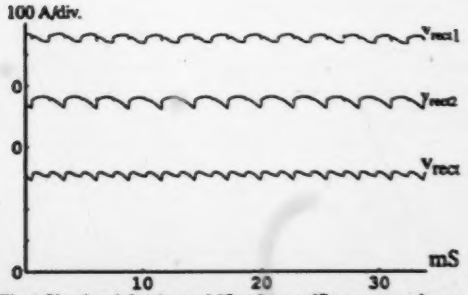


Fig.4 Simulated 6 pulse and 12 pulse rectifier output voltages

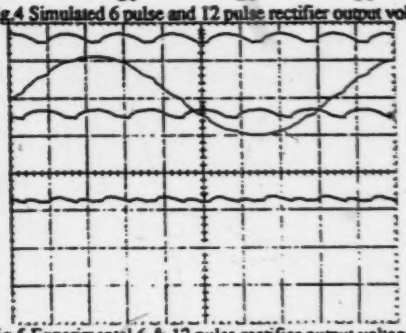


Fig.5 Experimental 6 & 12 pulse rectifier output voltages

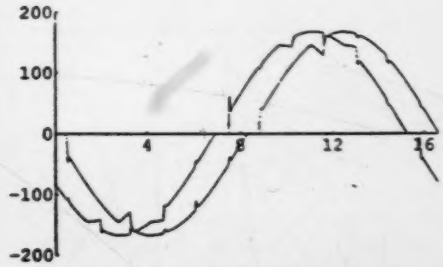


Fig. 6 Simulated ΔΔ and ΔY transformer secondary voltages

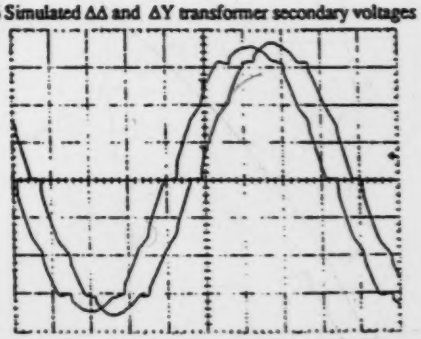


Fig.7 Experimental ΔΔ & ΔY transformer secondary voltages

4.VOLTAGE SOURCE INVERTER

The VSI is fed from a stiff DC voltage supply. Pulse Width Modulation (PWM) technique is used to obtain quasi sinusoidal current at the output of the inverter with the induction motor as the load. By comparing a triangular carrier wave with the fundamental frequency sine modulated wave, the natural points of intersection are obtained which determine the switching pattern of the power devices.

Each leg of the inverter bridge is modeled by a B function as shown in fig.8 defined as a product of two voltages, one representing the input DC voltage and the other the PWM switching pattern. The modeling of the six switching devices with three simple B statements simplifies the problem of a complicated circuitry, current commutation from one inverter leg to the other and reverse recovery problems of the diodes. A typical waveshape of the simulated and experimented phase voltage and current is shown in fig.9 and fig.10.

When the amplitude modulation ratio approaches unity, the notch-width near the center of the half-cycle tends to vanish. For satisfactory inverter operation, e.g. switching-aid circuitry, minimum pulse widths have to be maintained.

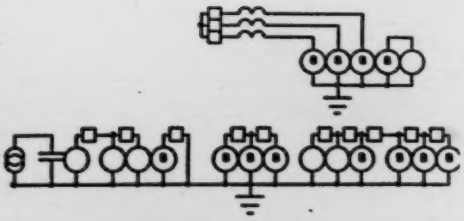


Fig.8 PWM-VSI: SPICE3 schematic

Fig.9 PWM-VSI: simulated phase voltage & load current

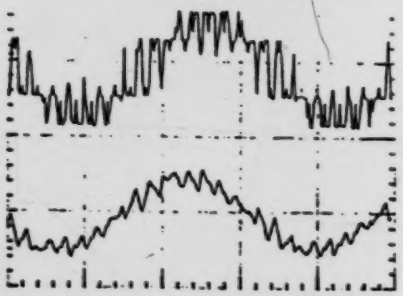


Fig.10 PWM-VSI: experimental phase voltage & current

5. CURRENT SOURCE INVERTER

The CSI can be supplied from an scr rectifier using a large DC-link inductor. The CSI is modeled in much the same way as the VSI with a capacitor bank at the input that makes the output current close to sinusoidal. Strictly speaking, any change in the machine impedance, with a change in slip, changes the magnitude of the DC-link current and the machine phase currents. In order to maintain the machine current independent of changes in machine operation, the DC-link current is maintained constant by closed-loop control. Simulated waveforms of the PWM-CSI are shown in Fig.11.

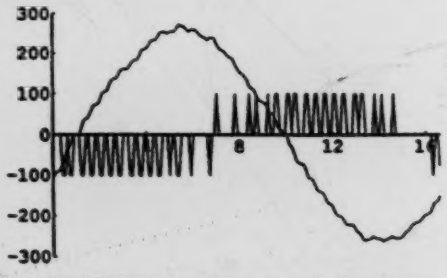


Fig.11 PWM-CSI: simulated line voltage & phase current

6. INDUCTION MOTOR

The induction motor is simulated using d-q axis models. The basic concept of modeling is very similar to that of a transformer.

The flux linkage expressions for the rotor in terms of the currents can be written as

$$\Psi_{qr} = L_r i_{qr} + L_m (i_{qs} + i_{qr}) \quad \ldots\ldots(6.1)$$

$$\Psi_{dr} = L_r i_{dr} + L_m (i_{ds} + i_{dr}) \quad \ldots\ldots(6.2)$$

These equations are used to model the rotor side of the motor.

The rotor side of both d and q schematics consist of a B-statement, which is a voltage function.

The d-axis voltage is function of the rotor and stator currents of the quadrature circuit. Similarly, for the q-axis, this voltage will be a function of the stator and rotor currents of the direct circuit.

The motor speed is related to the torque as

$$T_e - T_l = J\, d\omega_m/dt = {}^2/_p\, J\, d\omega_r/dt \quad \ldots\ldots\ldots\ldots (6.3)$$

where T_l is the load torque and J the system inertia.

The development of torque by the interaction of air gap flux and rotor mmf is given by

$$T_e = {}^3/_2 {}^*P/_2 {}^*\Psi_m \times I_r \quad \ldots\ldots\ldots\ldots\ldots\ldots (6.4)$$

or in terms of d-q components

$$T_e = {}^3/_2 {}^*P/_2 {}^*(\Psi_{dm}\, i_{qr} - \Psi_{qm} i_{dr}) \quad \ldots\ldots\ldots\ldots (6.5)$$

Considering the relations between fluxes and currents, the torque equation becomes

$$T_e = {}^3/_2 {}^*P/_2 {}^*L_m(i_{qs}\, i_{dr} - i_{qr}\, i_{ds}) \quad \ldots\ldots\ldots\ldots (6.6)$$

The equations (6.3) and (6.6) give the complete model of the electromechanical dynamics of the induction machine. The nonlinearity of the model is very evident. The obtained model using the transformation equations can be simulated for studying the transient and steady state performances. The above equations are implemented to model the output of the motor by using B-statement in parallel with a capacitor. The load (T_l) is simulated by a constant current source drawing current out of the capacitor.(fig.12).The capacitor in fact represents the system inertia (J). The B-statement models the torque T_e and is a function of the currents in the rotor and stator of the equivalent circuits. The voltage across the capacitor gives a measure of the rotor speed.

Fig.13 illustrates the simulated torque and speed with respect to time. The characteristic transient nature of the simulated stator current during the starting process of the machine is shown in fig.14 and is comparable with the experimental results shown in fig.15.

7. CONCLUSIONS

The various SPICE3 simulation techniques were implemented on the variable speed drive. The B statement simplifies the need of complex circuitry in the modeling of Power Electronic circuits. Thus reasonable run times can be achieved by a simple representation of remote parts of the circuit. Possible convergence problems were eliminated by avoiding the use of nonlinear micromodels of the power devices.

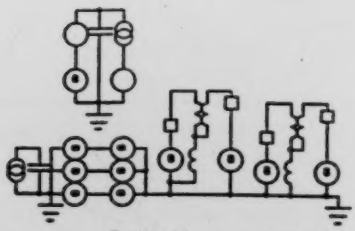


Fig.12 SPICE3 schematic for the Induction Motor (IM)

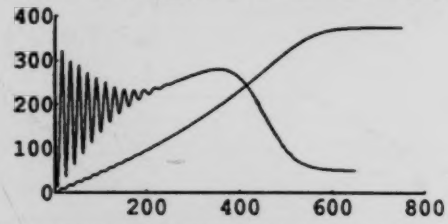


Fig.13 Simulated staring torque and speed curves for IM

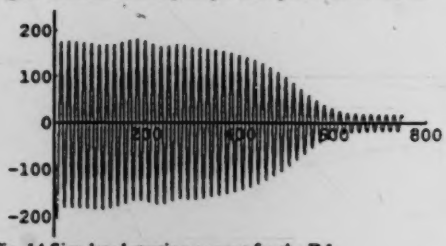


Fig. 14 Simulated starting current for the IM

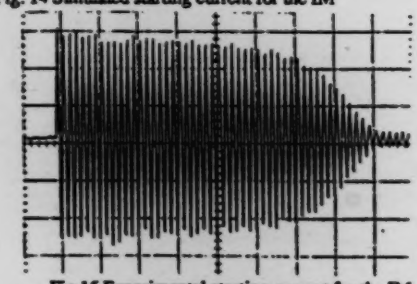


Fig.15 Experimental starting current for the IM

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SCR harmonic correction topologies for VSI drives

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Abstract

The circuit topologies described in this paper contribute to the technology of converting 3Ø ac power to dc, with the prime application being the input stage to commercial variable speed VSI drives. The converter topologies examined are essentially scr harmonic correction units (HCUs) suitable as a retrofit or as a drive option. The elementary HCU uses a 3-phase switch network to sequentially access each line voltage. Current pulses are drawn from the selected line voltage and low distortion line currents are drawn as a result. Each HCU topology has a hard switched and a resonant soft-switch version. Since the HCUs are separate to the main drive structure, drive operation can be maintain even if the unit fails, Alternatively, when low current thd is not required, the drive can be installed without the HCU to lower the drive cost. The performance of the power converters described in this paper are illustrated with reference to simulated and experimental data.

I. Introduction

This paper describes a series of techniques using thyristor switches that improve the harmonic content associated with the input current of diode rectifiers connected to a voltage sourced inverter drive. The topologies examined expand upon the 3Ø Y-switch network explored in recent articles [1-5], see Fig. 1(a). The 3Ø Y-switch network selectively shorts each rectifier input to the centre-tap of the dc rail. With ac line inductors present, this switching action draws current pulses from each line that results in improving the harmonic distortion of the total line current. A modified version of this topology in shown in Fig. 1(b) and consists of a 3-phase SCR "standard rectifier" switch network (3Ø SCR R-switch). This network is a low cost topology and performances the line voltage selection function, as described in [3]. The igbt or gto switch T_{ps} achieves control of the turn-on and the turn-off edge. Six low cost scr switches and 1 igbt switch replace the 6 igbt switches in the original circuit topology, see Fig. 1(a). The performance of the 3Ø SCR R-switch is very close to the original, with minor differences in the semiconductor conduction losses. Cost benefits are obtained together with improvements in the stability of topology.

A 3Ø scr resonant Y-switch, see Fig. 1(c), eliminates the need for a dc-rail centre tap and introduces soft-switching techniques. Control of the switch turn off edge is lost with the advantage of obtaining a low cost topology that is easily scaled in its power rating. A modification to this topology is the 3Ø scr resonant R-switch, see Fig. 1(d). The igbt switch allows control over the switch turn on and turn off. This improves the circuit controllability and adaptability to the p.u. power level.

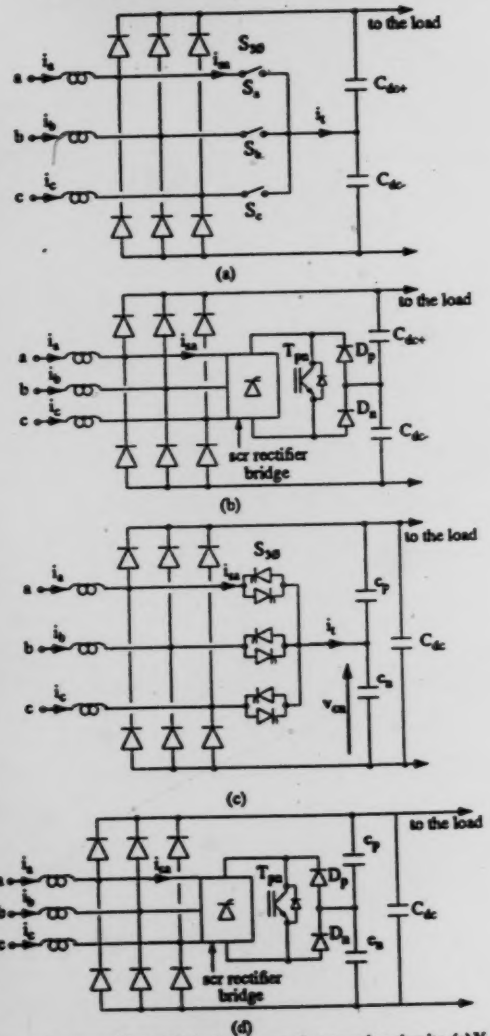

Fig. 1. Diode rectifiers with 3-phase harmonic correction circuits: (a) Y-switch & split dc-rail, (b) scr R-switch & split dc rail, (c) scr resonant Y-switch. (d) scr resonant R-switch.

II. Rectifier Operation

The operation of the rectifier topologies are described in this section with reference to the resonant switch topologies given in Fig. 1(c) and 1(d).

The scr resonant Y-switch, see Fig. 1(c), uses the scrs in the 3-phase switch network, $S_{3\phi}$, to build up the current in each phase prior to the normal conduction periods associated with a diode bridge rectifier. As a result, the harmonic distortion of the ac-line current can be lowered and the power factor lag associated with large line inductors is avoided.

To appreciate this resonant pulse action, consider the -ve to +ve zero voltage cross-over of the phase-a voltage with the cross-over point being defined as zero degrees. At -30° the current flowing through the phase-a diode is commutated by phase-b and the current in phase-a decays, see Fig. 2(a). The harmonic correction networks are not active in this period. At 0°, the positive scr in the Y-switch is turned on and current increases in phase-a, see Fig. 2(b). The voltage across C_p is initially E and C_n is zero. A resonant circuit is set up and the centre tap potential of the resonant capacitors increases up to the rectifier positive rail, see Fig. 2(d). The diode D_{a+} becomes forward biased and T_{a+} is naturally commutated, see Fig. 2(c). The circuit is now primed for the commutation of phase-c and the resonating action of lowering phase-c down to the negative. rail. The capacitor centre tap voltage, v_{cn}, and the resonant current pulse i_{pn}, is shown in Figs. 2(d) and 2(e) respectively.

The scr resonant Y-switch can define the starting edge of each current pulse but has no control over the negative edge or turn off period. In addition, the resonant capacitor centre tap potential is forced to traverse completely from the negative rail to the positive rail. This lowers the control options for the circuit switching action response to a wide load variation.

The scr resonant R-switch network uses an igbt, or gto switch, to define the turn on edge and turn off edge associated with the resonant action. The decay in the phase current at the edge of the diode bridge conduction period is not effected by this network and is the same as for the scr resonant Y-switch, see Fig. 3(a). The turn on edge to increase the current in phase-a is controlled by the turning on T_{pn} and a resonant pulse is set up, see Fig. 3(b). The turn off edge could be defiend by the centre tap potential of the resonant capacitors reaching the positive rail or defined exactly by turning off switch T_{pn}. Either way, the phase-a current transfers to the diode D_{a+} as shown in Fig. 3(c). The switch T_{pn} also controls the resonant pulse in the negative direction as illustrated in Fig. 3(d) for the increase in phase-c current in the negative direction.

The scr resonant Y-switch has the potentially for soft switching and for increased controllability in defining the resonant pulse. Referring to the resonant pulse associated with the -ve-to +ve zero cross-over of phase-a, the following control functions are possible: (a) turn on at 0° with a controlled turn-off time, (b) turn-off at 30° with a controlled turn on time, (c) switch on time centered at 15° with a variable on/off time, (d) switch on time centered at 30° with a variable on/off time. Some of these control strategies are investigated in the next section.

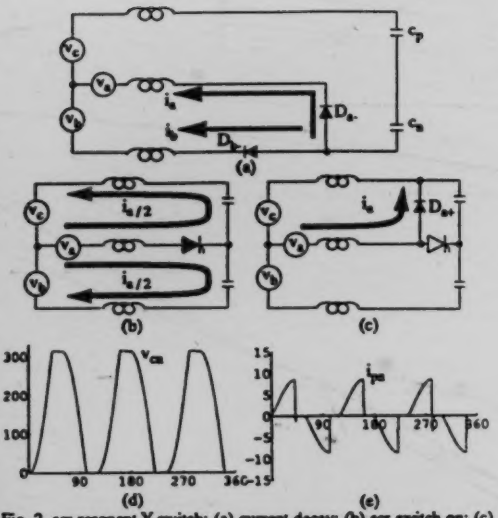

Fig. 2. scr resonant Y-switch: (a) current decay; (b) scr switch on; (c) scr commutation; (d) capacitor resonant voltage v_{cn}; (e) capacitor resonant current i_{pn}.

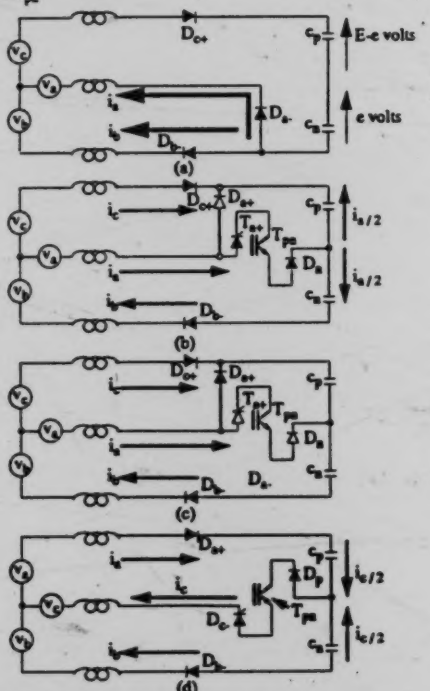

Fig. 3. scr resonant R-switch: (a) current decay in phase-a, (b)current ramp in phase-a, (c) commutation of the r-switch scr in phase-a, (d) current ramp in phase-c.

III. Rectifier Performance

This section describes some of the circuit design and control parameters that influence the operation of the harmonic correction topologies, namely the resonant capacitor size and the switch conduction periods. Spice 3 simulation results are used to obtain the various waveforms and performance curves in this section. The various features examined are considered with reference to the THD of the line current and the rectifier power factor. No consideration is given to control features or circuit designs that impact the size of the line inductors used.

(a) Waveforms

3-phase line currents obtained with the resonant scr Y-switch are shown in Fig. 4(a) with a setting that has the currents in phase with the phase voltages, see Fig. 4(b). This would normally only be achieved at the maximum power setting for the rectifier and using large inductors. The waveforms shown in Fig. 4(c) was obtained at a similar power level but using smaller line inductors. The line current is also typical of operation at lower per-unit levels if the circuit operating is optimized for the full power setting. The lowest line current thd is 5.4% and 14% using smaller inductors. With firing of the scrs at 0°, the line current distortion can get very high at low power levels.

Some improvement in the thd and power factor can be obtained by advancing the firing of the scrs from 0° up to 30° at very low power levels. Figs. 5(a) and 5(b) illustrate how the line current waveforms are effected by delaying the switch turn on by 12 ° but keeping the switch on time fixed at 30° [α_{on} =30°, α_{sw} = 12°]. This operation is only possible using the scr resonant R-switch network. Fig. 5(c) illustrates the rectifier performance using the same switching pattern and approximate power levels but smaller line inductors. The line current thd is still high but the power factor, relative to a diode bridge with similar line inductors, is improved.

(b) Performance Curves.

The scr resonant Y-switch was operated with a firing angle of 0°, α_{on} = 0°, and the resonant capacitor size changed, see Fig. 6. The line current THD is lowered initially, but as the capacitor size is increased further the curve flattens out .

The scr resonant R-switch was operated with a fixed resistor load and the switch on time was fixed and phase delayed: α_{on} = 30° & varying α_{sw}, see Fig. 7. The line current thd was lowered considerably around α_{sw}. The distortion changes its trend at low values of α_{sw} due to the line current not being reduced to zero at the end of each half cycle. This can clearly be observed in the rectifier power factor due to a lowering of the fundamental power factor.

The scr resonant R-switch was operated with a fixed resistor load with the switch on-time centered on 15° and varying the on-time, see Fig. 8. The line current thd is lowered the larger the on-time. The scr resonant R-switch was operated with a fixed resistor load with $\alpha_{sw/2}$ = 30°, and varying α_{sw}, see Fig. 9. The line current thd is lowered the larger the on-time.

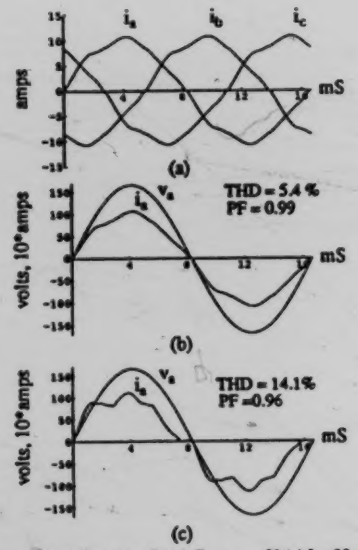

Fig. 4. scr resonant Y-switch: C=16μF, α_{sw} = 0°.(a) L_s=20mH, (b) L_s = 20mH, (c) L_s = 10mH

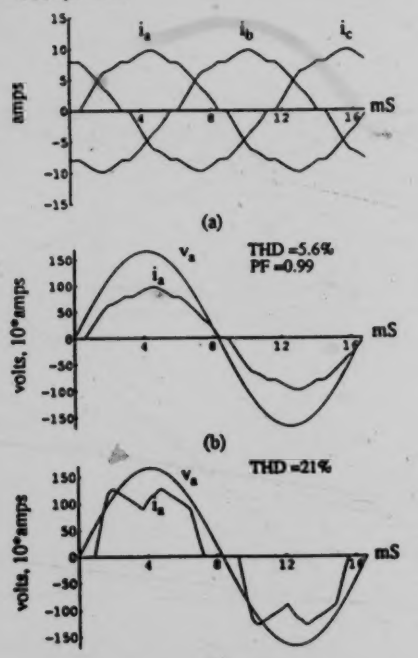

Fig. 5. scr resonant R-switch, C=16μF, α_{on} =30°, α_{sw} = 12°.(a) L_s=20mH, (b) L_s = 20mH, (c) L_s = 10mH.

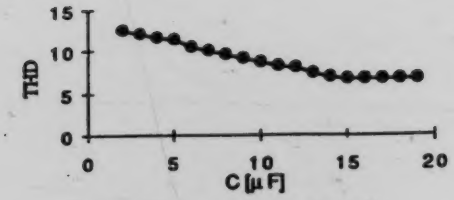

Fig. 6. scr resonant Y-switch : L=20mH

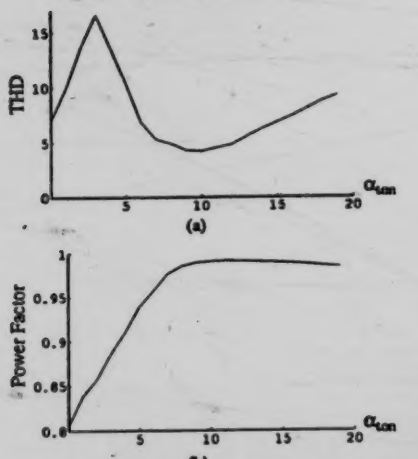

Fig. 7. scr resonant R-switch: α_{toff} = 30° & varying α_{ton} [L= 20mH, C= 16uH, P=2.2kW]

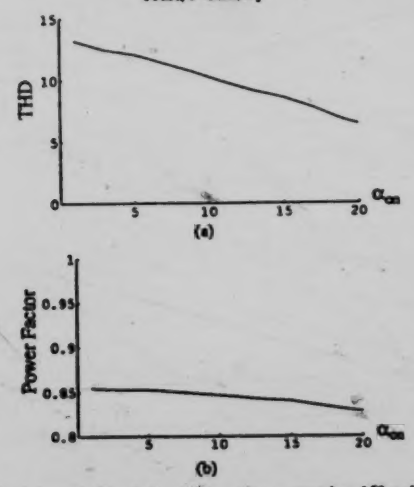

Fig. 8. scr resonant R-switch: switch on-time centered on 15° and varying the on-time [L= 20mH, C= 16μH, P=2.2kW]

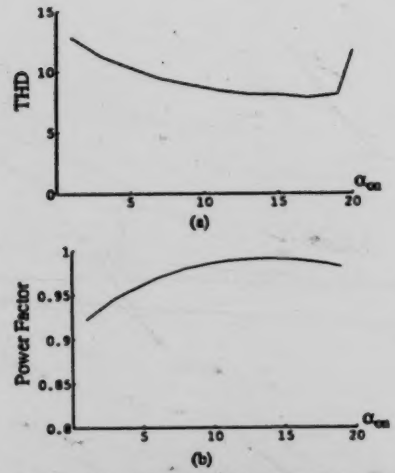

Fig. 9. scr resonant R-switch: α_{toff} = 30°, and varying α_{on} [L= 20mH, C= 16uH, P=2.2kW]

IV. Conclusions

The circuit techniques investigated increase the controllability of harmonic correction circuits that use scr switches and that draw pulsed currents from the 3-phase to improve the performance of a diode bridge. The low power ratings and electrical stresses associated with the switchmode converters make the harmonic correction units cheap, reliable and feasible as retrofits or as a drive option. The use of thyristors, together with the low switch low per-unit current ratings, make the HCU circuits suitable for a wide range of power levels.

V. Acknowledgments

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VI. References

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